Delta-Sigma Data Converters

Short Course

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Background and Significance

- Modern multimedia and communications systems entail digital signal processing with analog-to-digital or digital-to-analog conversion interfaces.
- Starting around 1990, Delta-Sigma began to replace other techniques for low-speed (<100kHz) and high resolution (>12 bits) data conversion.
- Today, every cell phone, iPod, CD / DVD player, TV, and PC LAN modem employs Delta-Sigma data converters!
- There are billions of them in the field, and chances are that you use them for many hours each day! You are carrying them around, they are in your home, in your office, in your car, everywhere you go! You listen to all music and phone conversations through them. They are part of processing your LAN / WAN and cellular signals, too.

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Background and Significance (2)

- In 1987, a top executive at AT&T Bell Labs told me that Delta-Sigma converters may never go into production. He said the subject had been researched for decades, there were too many unsolved problems, and they may not be economical!
- Research on this subject can be found as far back as the late 1940's (Phillips Labs – Delta modulators); research intensified in the mid-1960's, driven by Bell Labs, and then fell off after AT&T killed the 'Picture Phone' project. Research picked back up again in the early 1980's – the dawn of the digital multimedia and telecom era.
- In order for this technology to become viable, two things needed to happen: 1) COST: sub- 1 µm (after 1990); 2) idle tones had to be eliminated; 3) bandwidth and resolution needed to increase.

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Outline (1)

- Background and Significance
- Overview of Data Conversion Concepts
  - A/D, D/A, Quantization, Filtering
  - Oversampling Data Conversion
- Delta-Sigma Data Conversion
  - Noise Shaping
  - Overview of Topologies

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Outline (2)

- Advanced Topics
  - Idle Tones and Dithering
  - Stability
  - Higher-order 1-bit $\Delta\Sigma$M
  - Multi-bit $\Delta\Sigma$M with DEM or DAC Error Correction
  - $\Delta\Sigma$M with Continuous-time Loop Filters
  - Sampling Jitter
  - Pipeline or Continuous-Time Delta-Sigma (CT$\Delta\Sigma$)?
  - Bandpass and Quadrature $\Delta\Sigma$M
  - RF_2Bits and $Bits_2RF$
  - Fractional-N Phaselock Loops with $\Delta\Sigma$M
  - Applications
  - Digital Filtering: Decimation and Interpolation
- References

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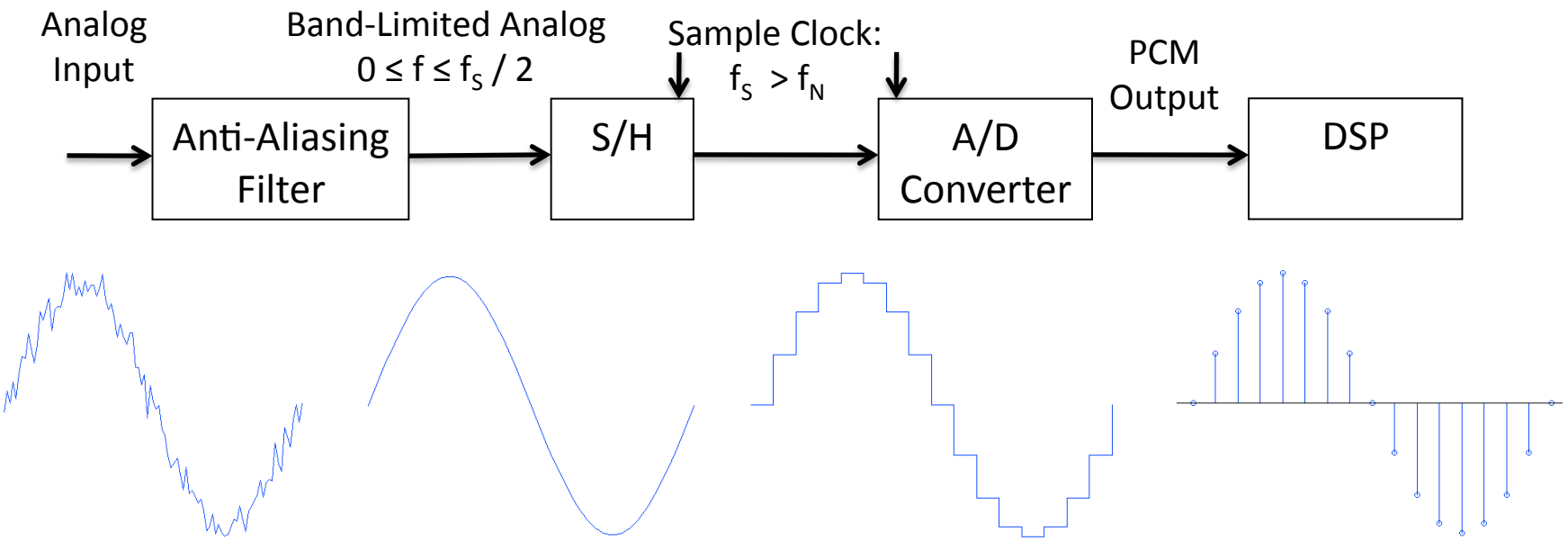
A/D Conversion



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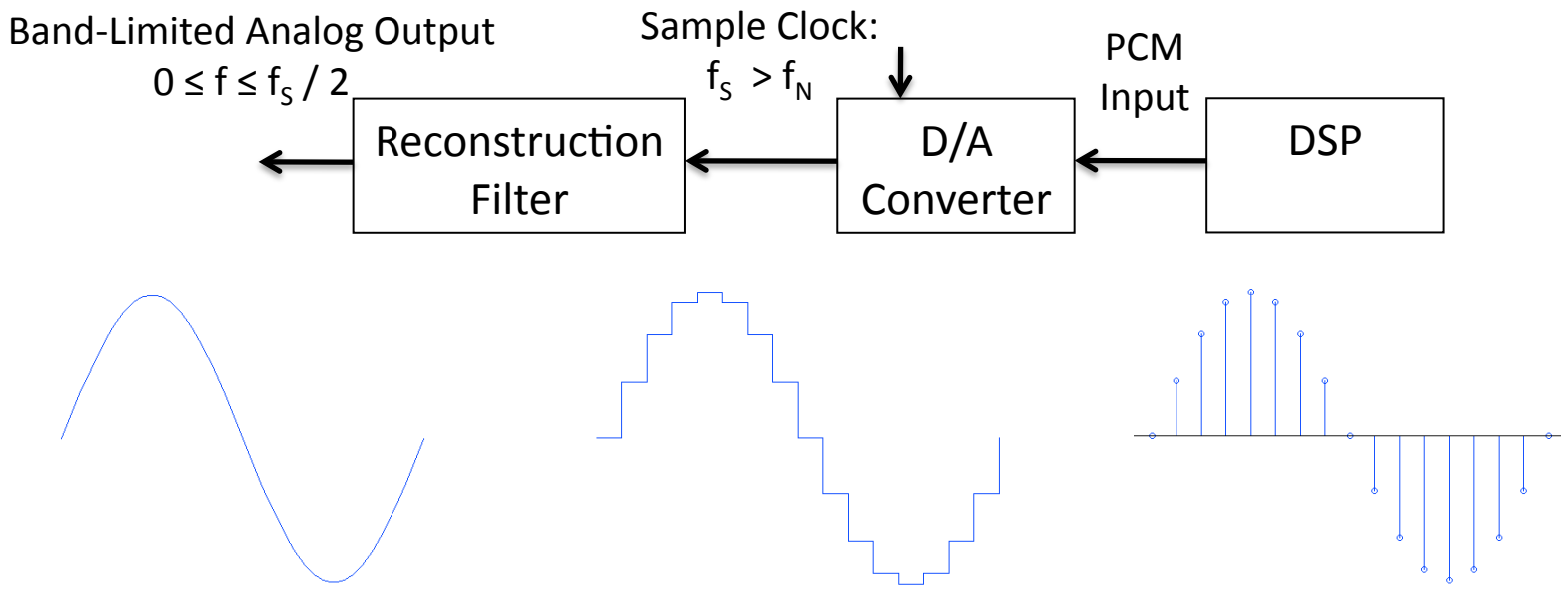
D/A Conversion



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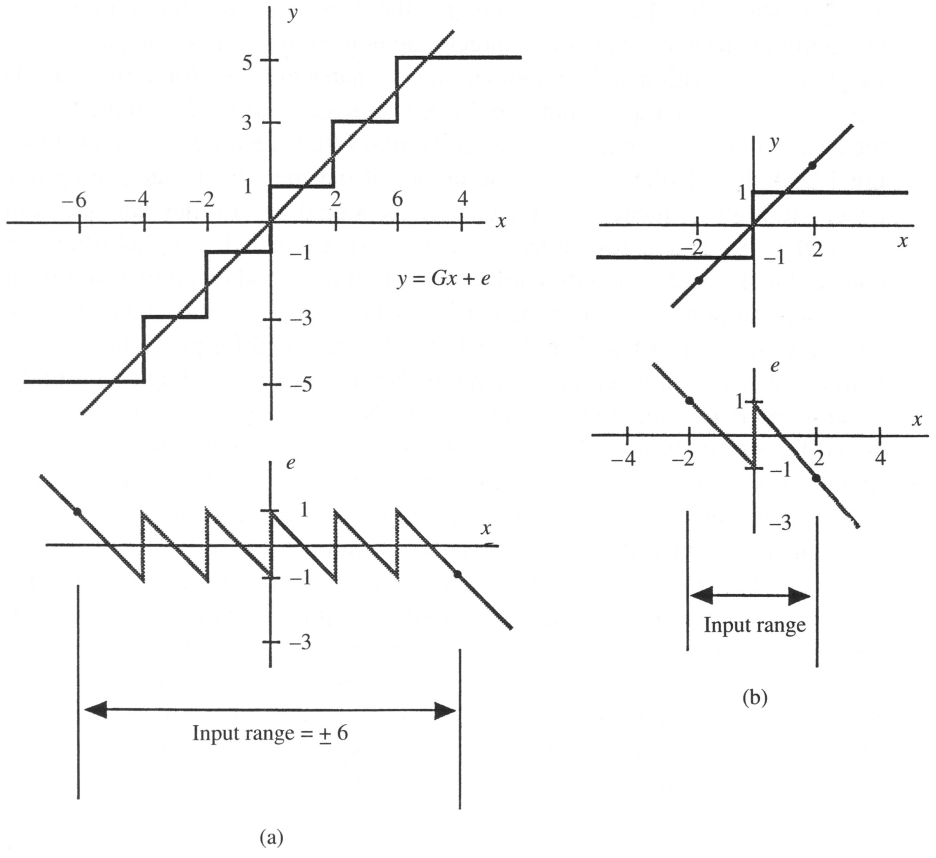
Quantization (1)

Central and critical to all A/D conversion techniques



(a) An example of a uniform multilevel quantization characteristic that is represented by linear gain G and an error e. (b) For two-level quantization the gain G is arbitrary.

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Quantization (2)

Assumptions:

1) quantization error is white and uncorrelated with the input, which requires RPDF dither spanning ±Δ/2
2) matching each quantization step size to within ±Δ/2 or less:
   Differential Nonlinearity (DNL) of $\leq \pm\Delta/2$
   Integral Nonlinearity (INL) of $\leq \pm\Delta/2$

$\sigma_e^2 =$ variance of $e =$ quantization noise power

$$\sigma_e^2 = E[(e - m_e)^2] = E[e^2] - m_e^2$$

$$E[e^2] = \int_{-\infty}^{\infty} e^2 p(e)de = \int_{-\Delta}^{0} \frac{e^2}{\Delta} = \frac{\Delta^2}{3}$$

$$m_e = \int_{-\infty}^{\infty} ep(e)de = \int_{-\Delta}^{0} \frac{e}{\Delta} = -\frac{\Delta}{2}$$

$$\sigma_e^2 = \frac{\Delta^2}{3} - \left(-\frac{\Delta}{2}\right)^2 = \frac{\Delta^2}{12} = \frac{2^{-2b}}{12}$$

$$SNR = \frac{\sigma_x^2}{\sigma_e^2} = \frac{\sigma_x^2}{2^{-2b}/12} = \frac{\text{Signal Power}}{\text{Quantization Noise Power}}$$

$$SNR(dB) = 10\log_{10}\sigma_x^2 - 10\log_{10}\left(2^{-2b}/12\right)$$

$$= 10\log_{10}\sigma_x^2 + 6.02b + 10.79$$

For a sinusoidal input, $x(t) = A_o \sin \omega t$,

$-0.5 \leq A_o \leq 0.5$

$\sigma_x^2(\max) = E[x^2(t)] = A_o^2/2$ (since $m_x = 0$)

$$SNR_{\max}(dB) = 10\log_{10}(0.5^2/2) + 6.02b + 10.79$$

$$SNR_{\max}(dB) = 1.76 + 6.02b$$

For $b = 16$, $SNR_{\max}(dB) = 98.09\ dB$

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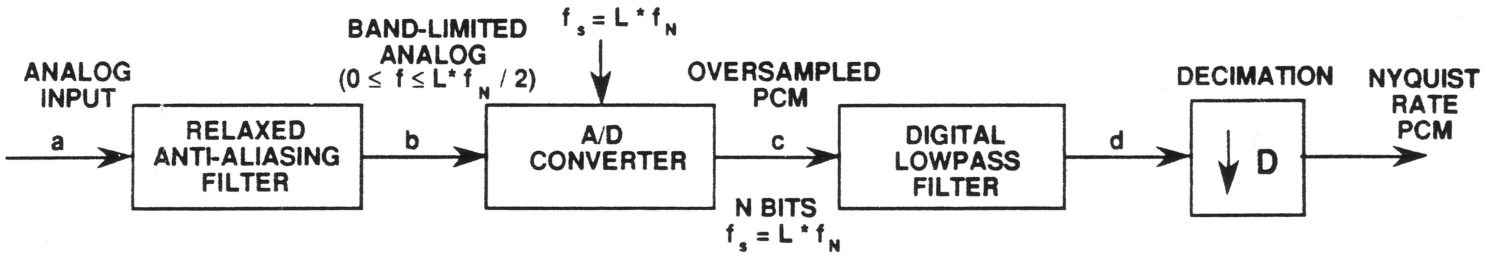
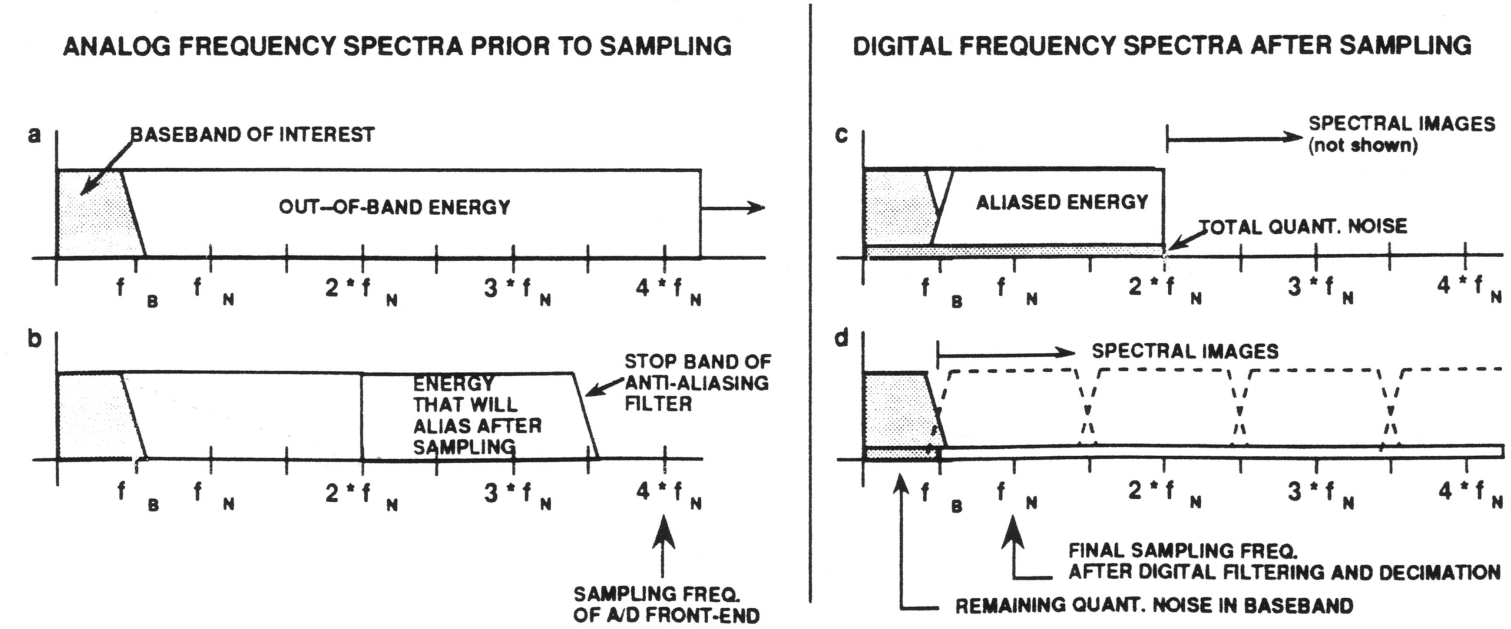
Oversampled A/D Conversion (1)



EXAMPLE: D = 4 TIMES OVERSAMPLING



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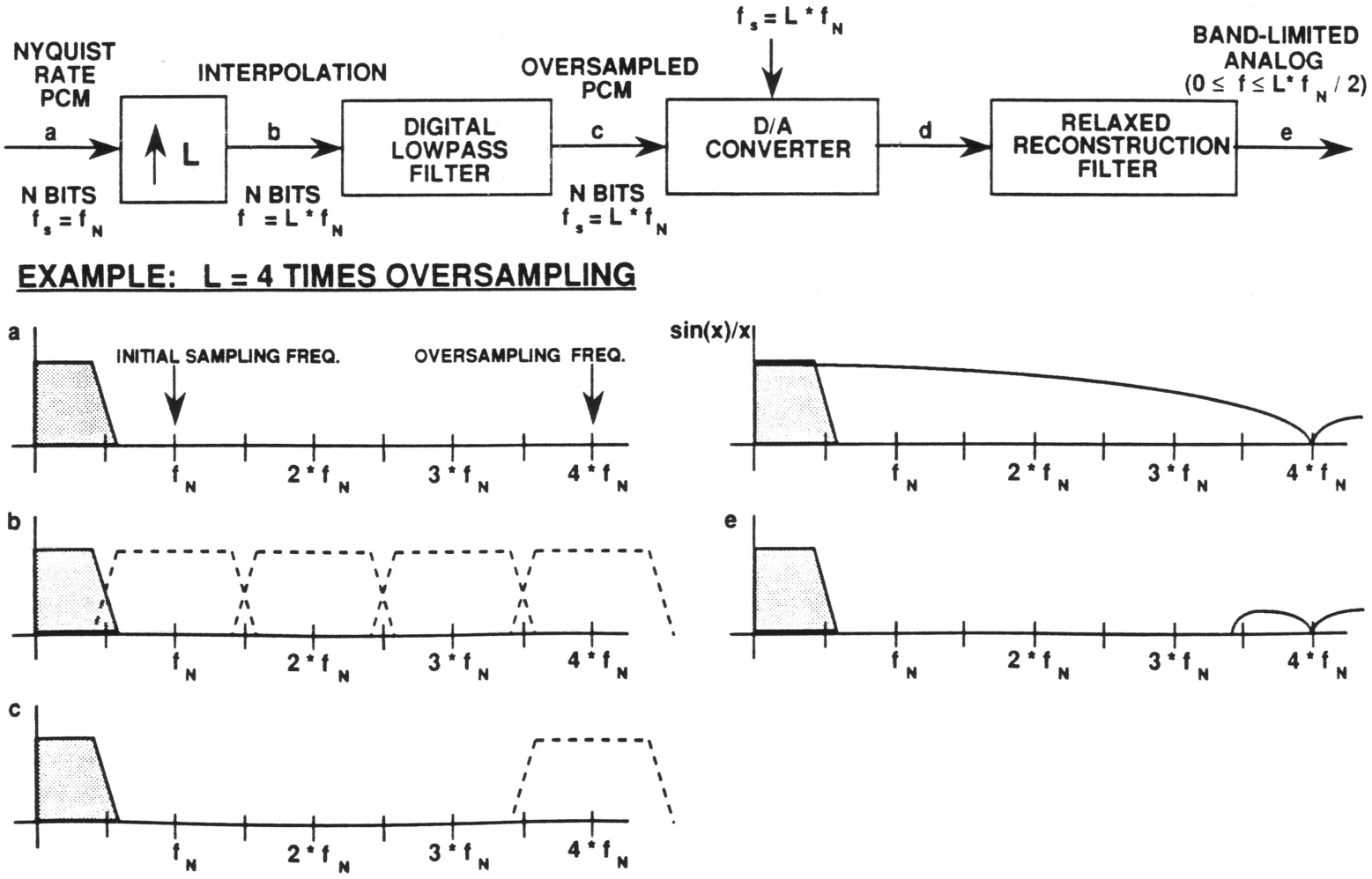
Oversampled D/A Conversion (2)



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Benefits of Oversampled A/D

- Quantization noise in band is inversely proportional to the oversampling ratio, resulting in ½-bit (3.01 dB) improvement in resolution for every factor of 2 higher sample frequency,
- (which assumes that the quantization error is white and uncorrelated with the input, which requires RPDF dither spanning $\pm\Delta/2$)
- Anti-aliasing filters are relaxed, resulting in more linear phase and less *sin(x)/x* droop in band.

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Quantization Noise Shaping

- Oversampling by itself only spreads out the quantization noise evenly across all frequencies.
- However, the basic concept behind noise shaping is to take the quantization error and highpass filter it, pushing most of the noise out of the baseband of interest.
- The first known description of this was in a Bell Labs patent filed in 1952 by Cutler. A few years later, the Delta-Sigma Modulator was described, also accomplishing noise shaping.
- Today, there are many variant architectures in practice that employ the basic principles of oversampling and noise shaping.

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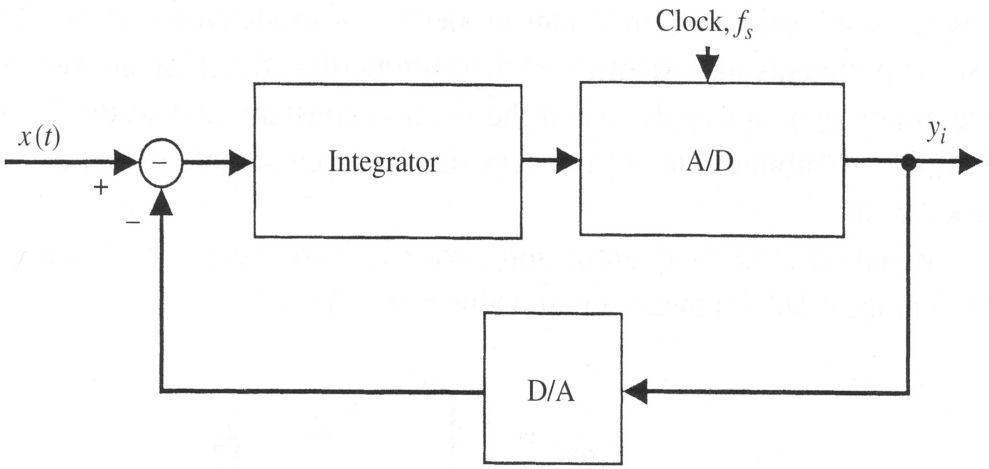
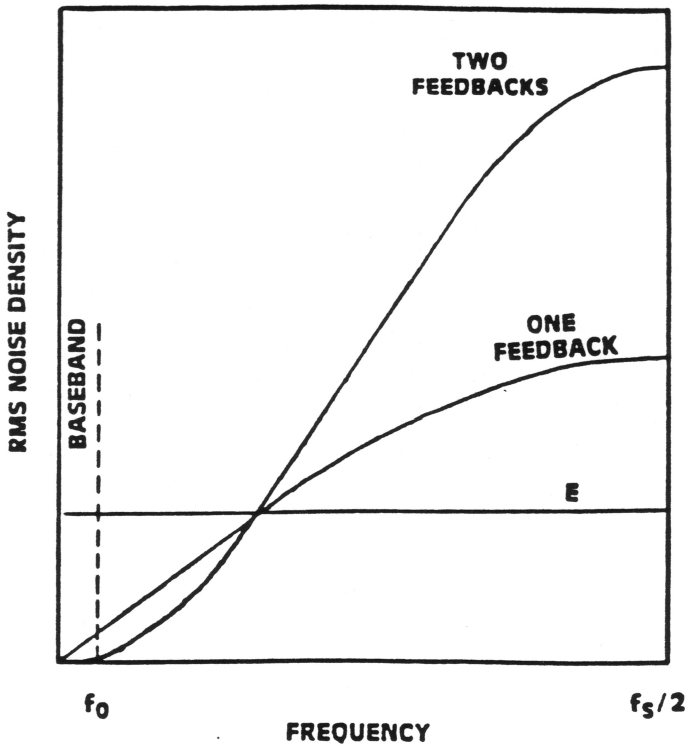
ΔΣ Modulator: Basic Concept





Integration or Lowpass Filtering in the Forward Loop Filter Causes Differentiation or Highpass Filtering of the Quantization Error Through the Use of Feedback

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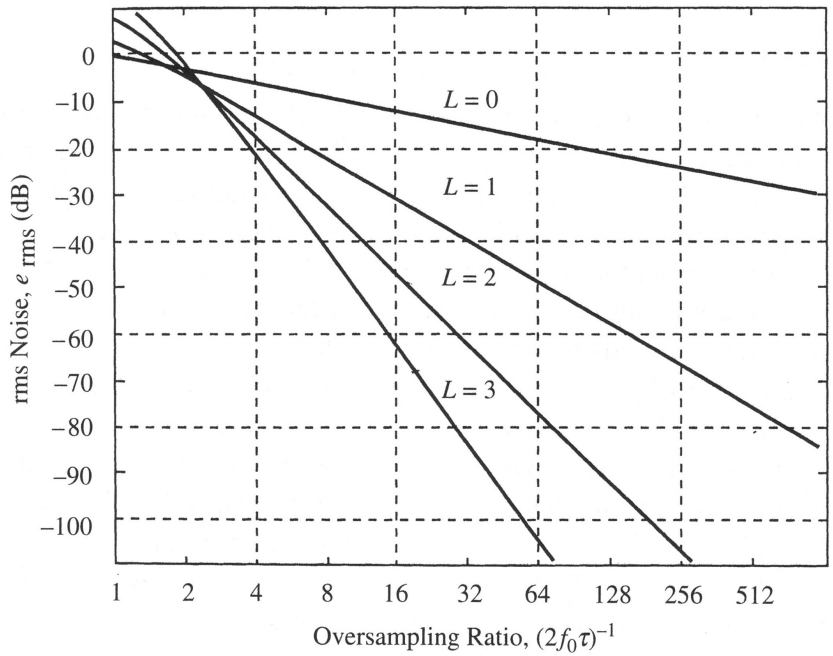
Resolution vs. Complexity

For oversampling ratios greater than 2, the rms noise in the signal band is given approximately by

$$n_0 = e_{\text{rms}} \frac{\pi^L}{\sqrt{2L+1}} (2f_0T)^{L+1/2}$$

This noise falls $3(2L-1)$ decibels for every doubling of the sampling rate, providing $(L-\frac{1}{2})$ extra bits of resolution, but we shall see that there are difficulties in implementing circuits containing more than two integrators.



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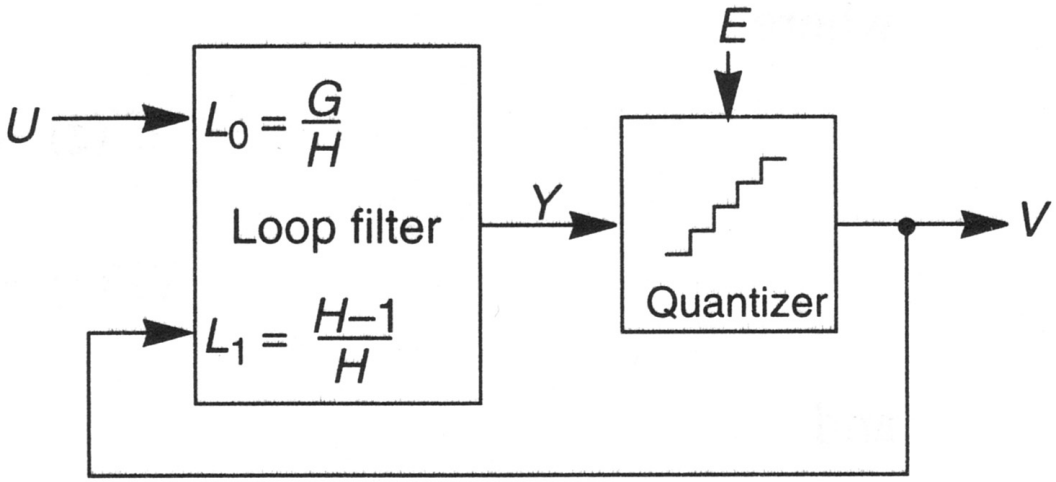
Noise Shaping Topologies (1)

Define a general structure and framework to map any given topology into.



A two-input one-output system, where L_o filters the input *U*, and L_1 filters the output *V*, which is then fed back. The linear combination is then quantized by *Q*, which forms the output. From the diagram, one can readily derive the following relationships:

NTF (Noise Transfer Function)
STF (Signal Transfer Function)

$$V(z) = STF(z)U(z) + NTF(z)E(z)$$

$$NTF(z) = \frac{1}{1 - L_1(z)}$$

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)}$$

$$L_0(z) = \frac{STF(z)}{NTF(z)}$$

$$L_1(z) = 1 - \frac{1}{NTF(z)}$$

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Noise Shaping Topologies (2)

- Error Feedback Only
- 1^{st} – and 2^{nd} – Order Loops with pure integrator(s) and 1-bit quantizer
  - The original $\Delta\Sigma$ modulator, but now less popular
- Cascaded stages (multiple quantizers).
- Higher-order non-monotonic loop filters with a single quantizer.
- Multi-bit quantizers with mismatch shaping.
- Continuous-time (vs. discrete-time) loop filters
- Bandpass $\Delta\Sigma$ modulators

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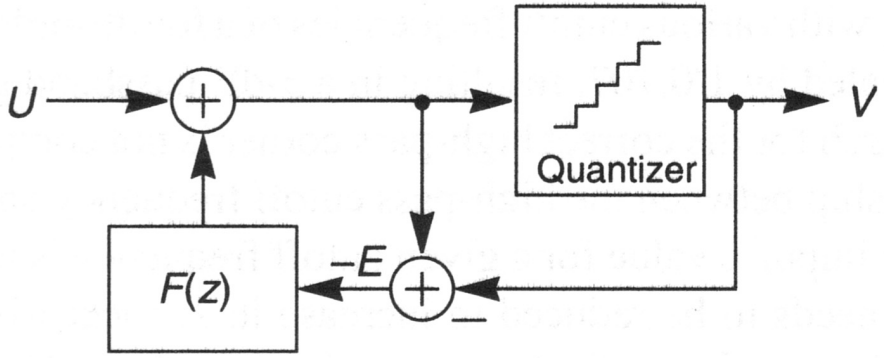
Error Feedback Only



$$STF = 1$$
$$NTF = 1 - F(z)$$

This topology is imposing no STF whatsoever, and only shaping the quantization error. It is essentially the simplest concept in noise shaping, and is basically what Cutler filed in his 1952 patent!

It is of little practical consequence in analog (A/D) implementations, but is commonly used D/A design where the error shaping is all digital.

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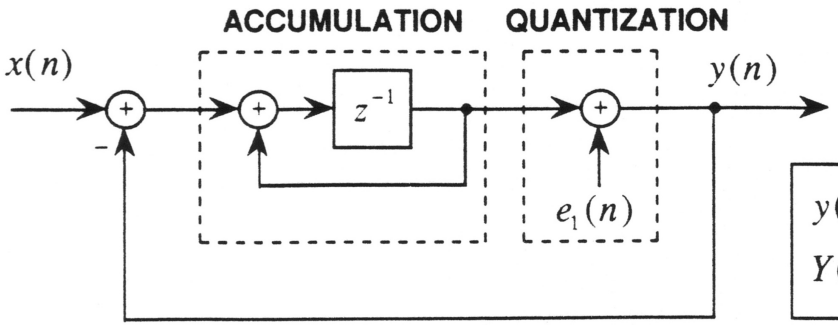
1st - and 2nd - Order ΔΣ Modulators

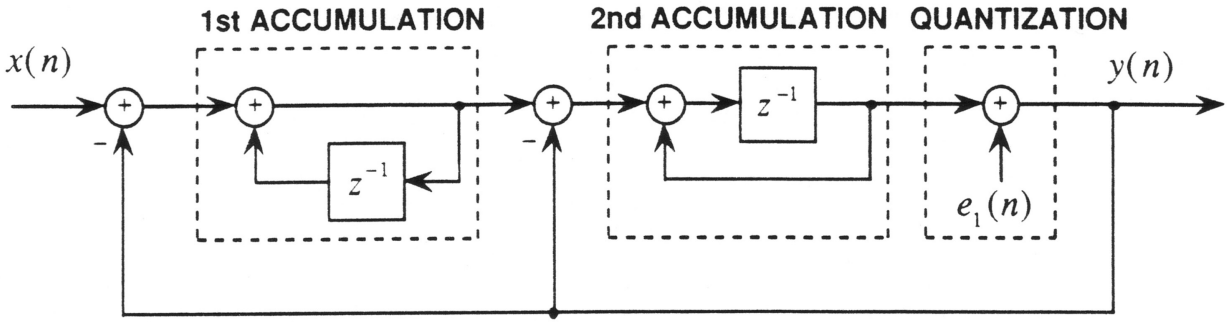
1st - Order ΔΣ Modulator



$$y(n) = x(n-1) + e(n) - e(n-1)$$
$$Y(z) = X(z)z^{-1} + E(z)(1-z^{-1})$$

$NTF = 1 - z^{-1}$
$STF = z^{-1}$

2nd - Order ΔΣ Modulator



$$y(n) = x(n-1) + e(n) - 2e(n-1) + e(n-2)$$
$$Y(z) = X(z)z^{-1} + E(z)(1-z^{-1})^2$$

$NTF = (1 - z^{-1})^2$
$STF = z^{-1}$

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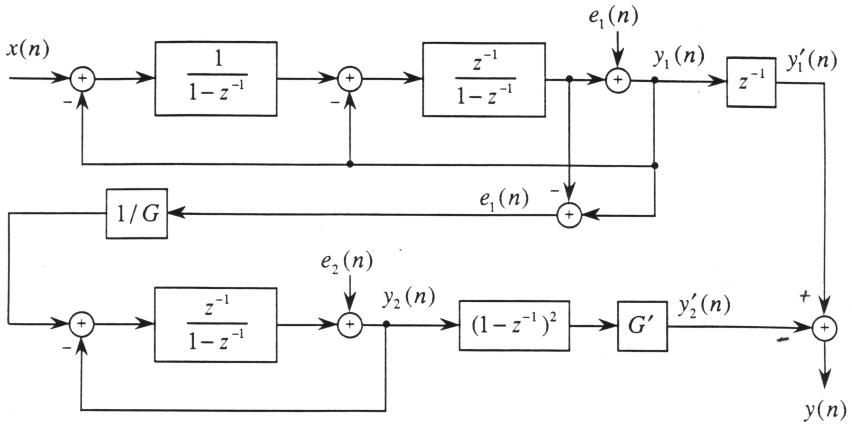
Cascaded Stages



$$Y_1(z) = X(z)z^{-1} + E_1(z)(1-z^{-1})^2$$

$$Y_2(z) = \frac{E_1(z)}{G}z^{-1} + E_2(z)(1-z^{-1})$$

$$Y_1'(z) = X(z)z^{-2} + E_1(z)(1-z^{-1})^2 z^{-1}$$

$$Y_2'(z) = E_1(z)\frac{G'}{G}(1-z^{-1})^2 z^{-1} + E_2(z)G'(1-z^{-1})^3$$

$$Y(z) = X(z)z^{-2}$$

$$+E_1(z)(1-z^{-1})^2 z^{-1} - E_1(z)\frac{G'}{G}(1-z^{-1})^2 z^{-1} \rightarrow \text{Residual 2nd-order noise}$$

$$-E_2(z)G'(1-z^{-1})^3 \rightarrow \text{3rd-order noise}$$

Example:

2nd–order ΔΣM followed by a 1st–order ΔΣM

The quantization error from the 2nd–order ΔΣM is passed into the proceeding 1st–order ΔΣM and then the 2nd–order NTF is digitally imposed on the output and subtracted from the output of the first ΔΣM, resulting in 3rd–order noise shaping.

Issue: gain matching between analog and digital.

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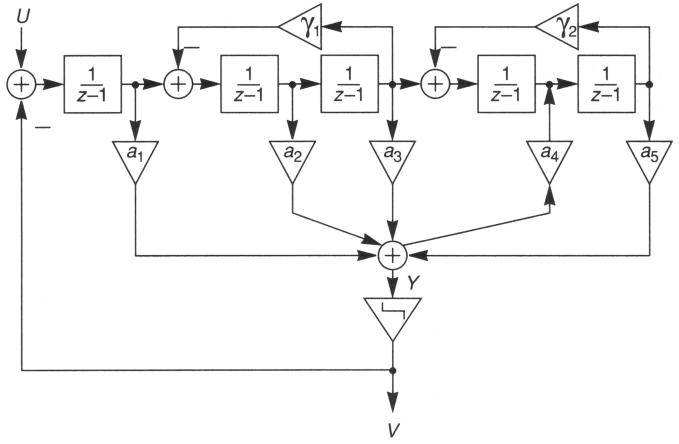
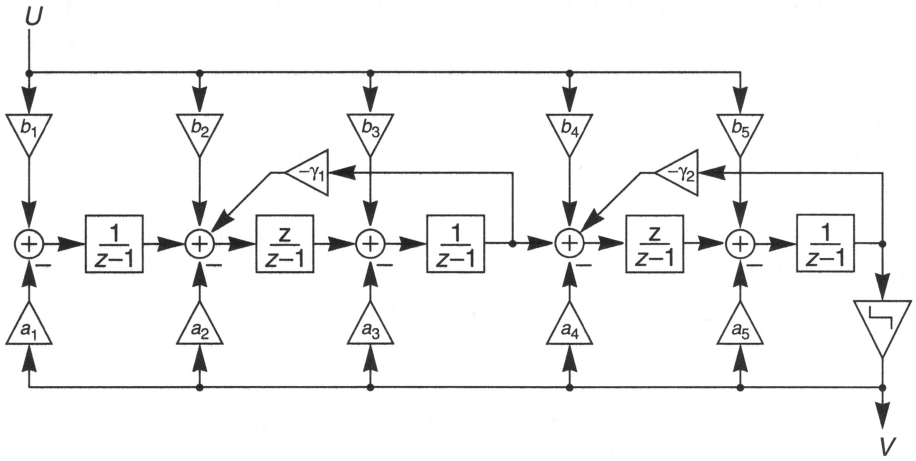
Higher-order non-monotonic loop filters with a single-bit quantizer



Chain of integrators with feedforward summation and local resonator feedbacks and a single feedback path from quantizer.



Chain of integrators with distributed feedforward input paths and local resonator feedbacks and multiple feedback paths from quantizer.

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Tones and Dithering (1)

- All ΔΣM's are subject to tonal behavior to some degree. Tonal behavior is well documented in the literature, as are solutions.
- Incorporated by reference:
  - Ch. 3 of Delta-Sigma Data Converters. Norsworthy, et al. IEEE Press. 1997.
- Despite this, the subject is still widely misunderstood.
- Whether or not tonal behavior is a problem is dependent on:
  - The architecture of the ΔΣM:
    - Order (higher is better); Number of bits (higher is better)
    - NTF type (pole/zero locations): higher out-of-band gains are better
    - Multi- vs. single-stage: multi-stage is better
  - Intermodulation and tone folding into baseband can occur due to:
    - Nonlineaities in the design - difficult to predict and simulate.
    - Clocking demodulation - also difficult to predict and simulate.
    - High-power out-of-band input signals – receiver design beware!
  - In CT designs, the problem is worse:
    - When the out-of-band gain is low due to RC and gain variation, tones start rising up due to poor suppression of quantization noise.

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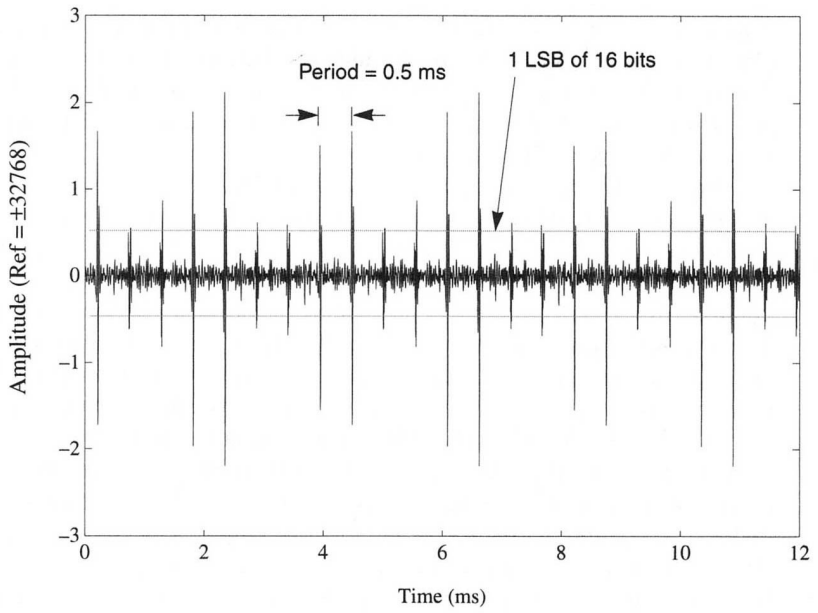
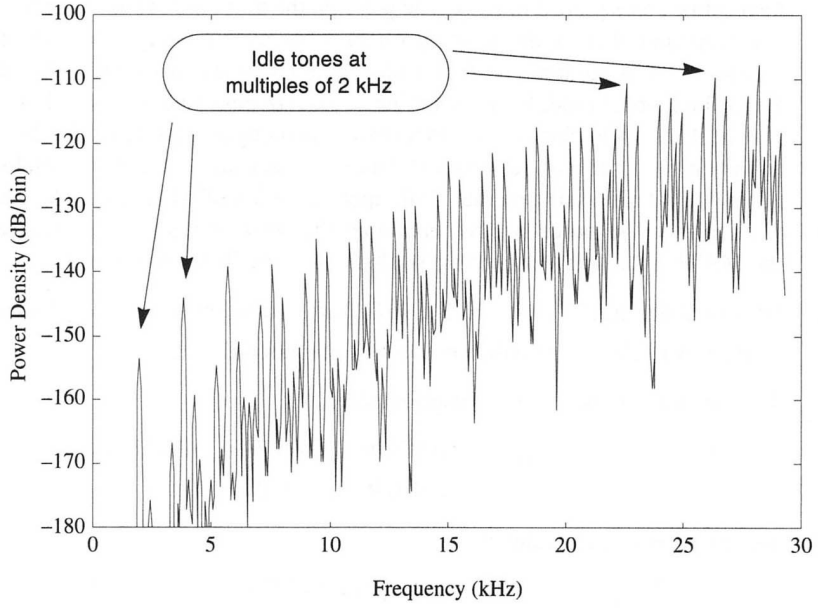
Tones and Dithering (2)

- Most of the early classic ΔΣM's were 1-bit designs. These fundamentally produce periodic tonal patterns.
- These tonal patterns have a very high Peak-to-RMS ratio. They are often seen as periodic impulse train patterns in the time domain, making them hard to find using spectral analysis alone. The human ear is a very good peak detector and can pick out these patterns easily, especially during silence in music or speech applications.



Low-pass filtered time output of third-order single-stage modulator for dc input. All three zeros at 0 Hz.



Baseband spectrum of third-order single-stage modulator for dc input. All three zeros at 0 Hz.

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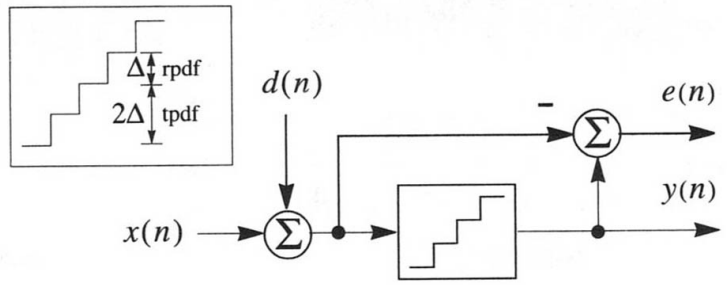
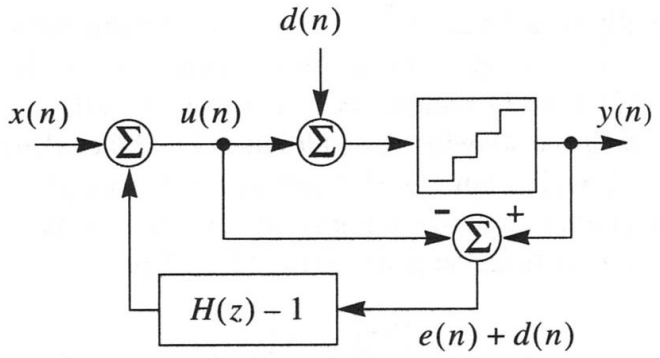
Tones and Dithering (3)

- Dithered quantization is a subject that has its origins in the 1950's. The error of any quantizer is not white but correlated with the input. The problem is far worse for ΔΣM because of the feedback and quantizer overloading.
- The only good way to eliminate the tones in ΔΣM is by noise-shaped dithering.
- Noise-shaped-dithered ΔΣM was invented by Norsworthy in 1989 at Bell Labs.
- This solution helped enable the commercial acceptance of ΔΣM in voice and audio codecs without resorting to higher-order ΔΣM or more costly architectures.
- The simplest way to achieve noise-shape dither is by inserting dither at the quantizer input.



PCM quantization with dithering.



General noise-shaping coder with dither.

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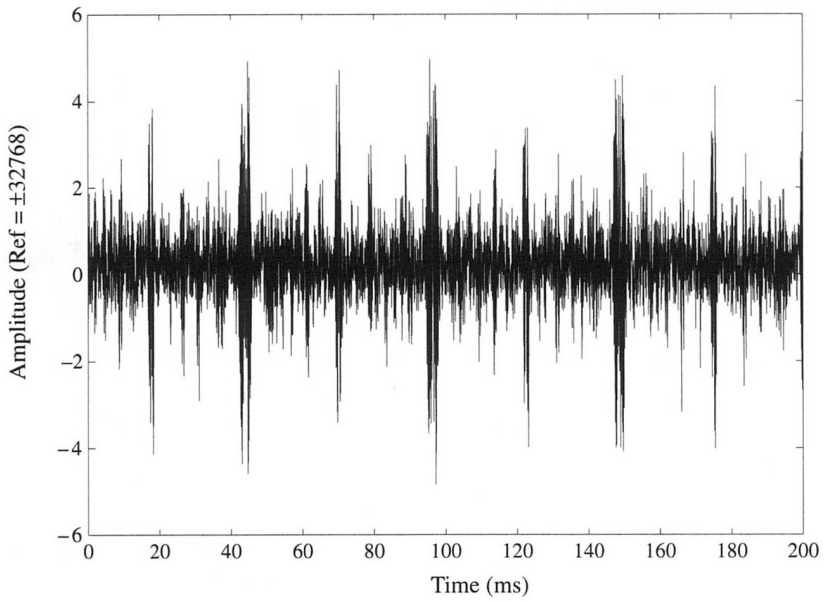
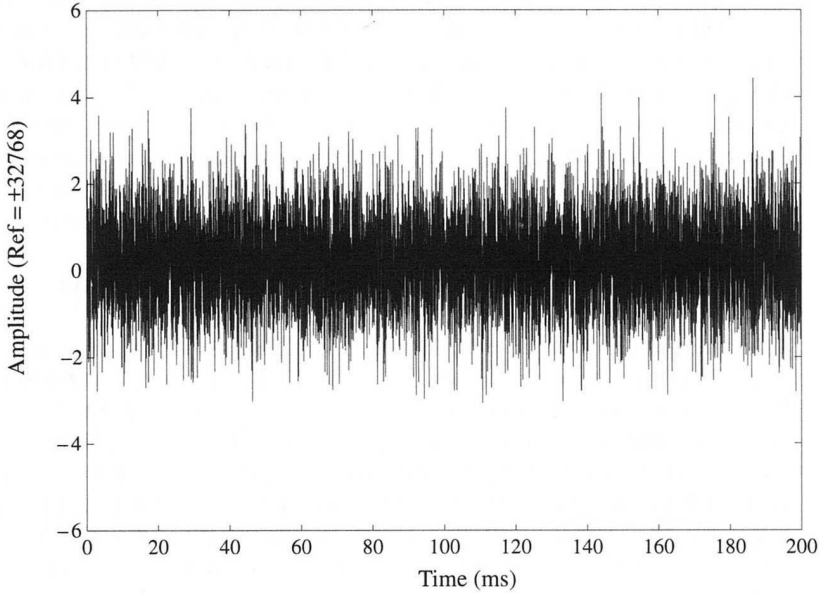
Tones and Dithering (4)

The power level of the dither is critical. In order to keep from driving the quantizer into gross overload, the dither cannot span more than about ½-LSB of the quantizer, which is just enough to decorrelate most of the tonal patterns. This is a practical solution, is very easy to implement, and incurs insignificant cost or hardware.



Captured time-domain output from undithered second-order ΔΣ D/A converter chip.



Captured time-domain output of dithered second-order ΔΣ D/A converter chip.

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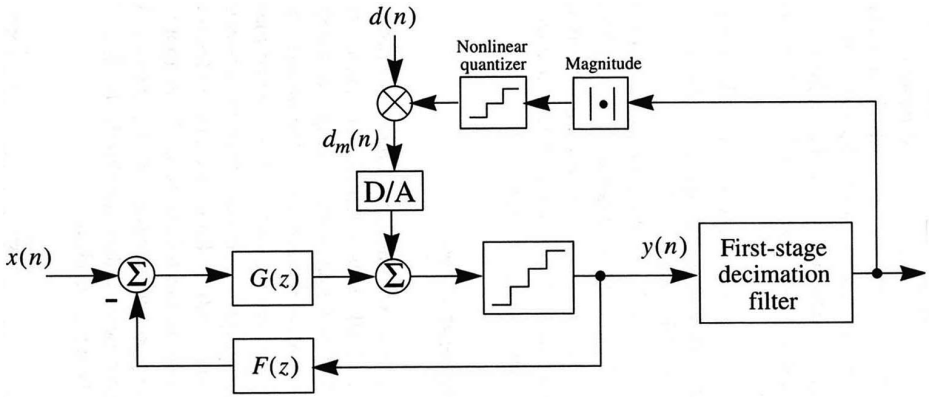
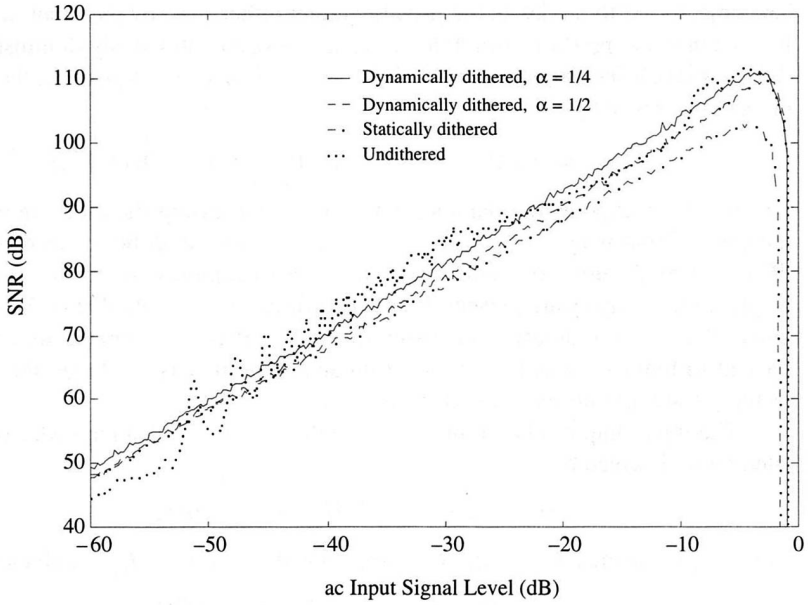
Tones and Dithering (5)

The useful top-end of dynamic range is reduced because the quantizer overloads sooner with the added dither signal. This can be overcome by reducing the dither as the input signal gets larger. This concept was invented by Norsworthy in 1992 at Bell Labs was called Dynamic Dither. It was commercialized by Texas Instruments for SACD audio.



A ΔΣ A/D converter with dynamic dither, having input signal magnitude estimate taken digitally at the output of the first-stage decimation filter.



SNR vs. ac input signal level for dynamically dithered, statically dithered, and undithered third-order modulator.

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Stability (1)

- All 1-bit ΔΣM's of order > 2 are subject to unstable behavior. By unstable, we mean that without a nonlinear control, the modulator may go into an unrecoverable oscillatory state.
- The quantizer does not have enough dynamic range to 'contain' the large amount of out-of-band gain of quantization noise without saturating. Once the quantizer saturates, the quantizer feeds back an estimate that no longer represents the proper linear state, which self-perpetuates with positive feedback and causes a unstable low frequency oscillation to occur, from which it cannot recover.
- Solution: design the NTF filter such that the maximum out-of-band gain is limited by the Lee Criterion:

A binary ΔΣM with an *NTF = H(z)* is likely to be stable if $\max_{w} \left| H(e^{jw}) \right| < 1.5$

- Additionally, use an NTF highpass filter design containing stopband zeros, such as a Chebyshev Type-II characteristic, suppressing the quantization noise in the region of interest with equiripple (constant weighting), allowing for a flat out-of-band gain over a broad region.

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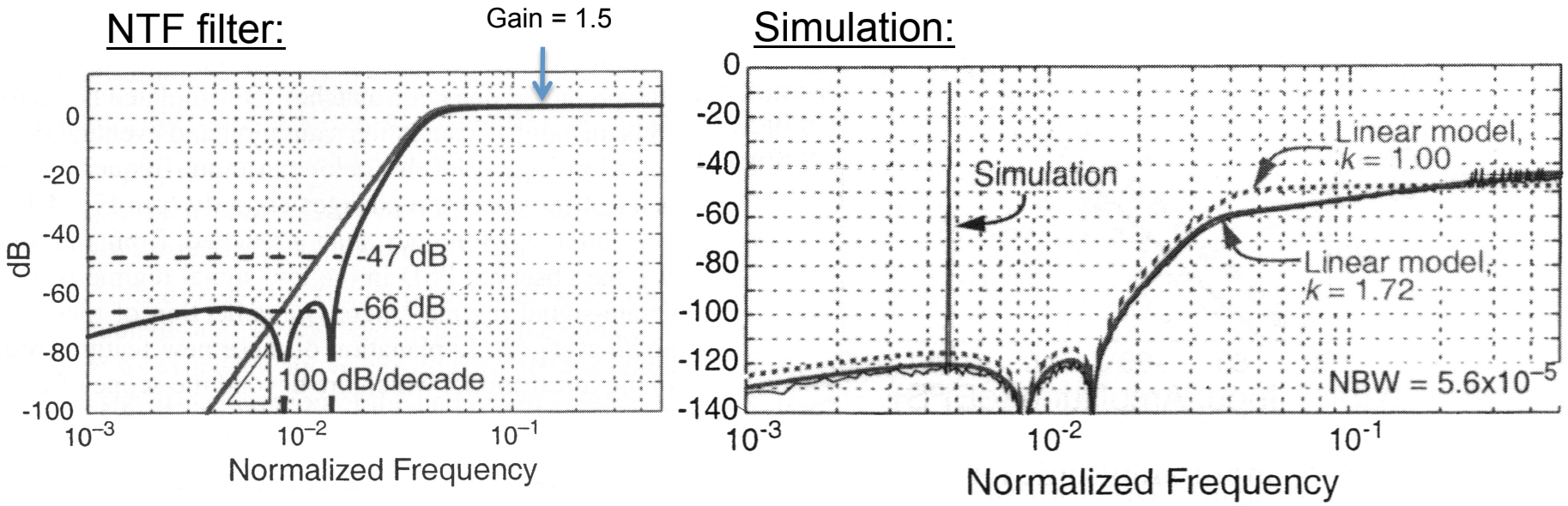
Higher-order non-monotonic loop filters with a single-bit quantizer (2)



Example NTF has similar characteristic of Chebyshev-II highpass filter; by optimizing the placement of the zeros and limiting the maximum out-of-band gain, *G*, by the Lee Criteria of 1.5, it has superior suppression of the quantization error in the signal band and it remains stable if the input level remains low enough to prevent quantizer saturation.

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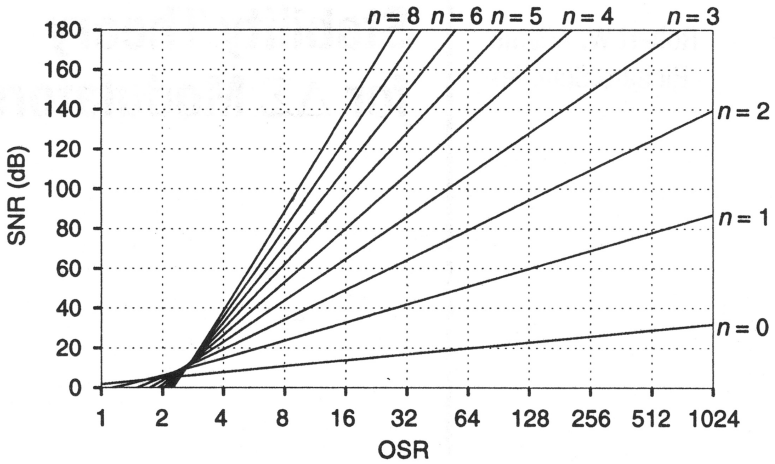
Higher-order non-monotonic loop filters with a single-bit quantizer (3)

Motivation:

Pure integrator-base loops of order > 2 with single-bit quantizers are unstable.

An alternative to cascaded stages.

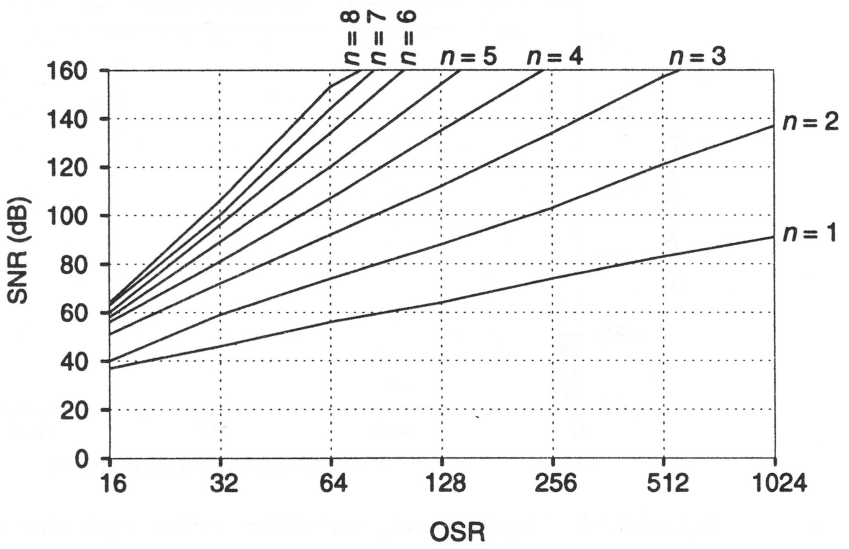


Theoretical SNR of a $(1-z^{-1})^n$ modulator vs. the oversampling ratio for $n = 0, \ldots, 8$. High-order modulators achieve very high SNR at moderate values of OSR.

UNSTABLE

Benefits:

Solves the gain matching problem while preserving the benefit of single-bit quantizer



Maximum SNR achieved by modulators of order n whose zeros have been optimally spread across the band of interest.

STABLE (with nonlinear control)

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Stability Control (1)

- With the Lee Criterion, now there is enough dynamic range to 'contain' the quantization noise, but not enough to 'contain' the input signal to full scale.

- Empirical methods and simulations can be used to predict the maximum input signal amplitude before instability. Typically, this will be about $1/G$ of the Lee Criterion, or approximately 0.6 times full scale.

- Two nonlinear stability control methods have been reported in the literature:

  - Controlled saturation of the integrators. This is an analog technique. By simulation, we first determine an analog value to which that we clamp.
  - Instability detection, followed by integrator reset. Can be implemented by counting the number of successive ones or zeros at the modulator output: too many, then instability is assumed, and the integrating capacitors are cleared (shorted out) with a reset switch.

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Stability Control (2)

- Newer method:
  - Set a programmable register value at the output of the first decimator.
  - Then compare it to each sample output of the decimator (at the decimated rate).
  - If the value exceeds the register value, both the integrators as well as the decimator flip-flops are reset.
  - Each reset occurrence may be reported and accumulated in a register history file for debugging purposes.
  - Can force the modulator into reset BEFORE instability occurs if desired.
  - May select parameters that raise or lower the instability sensitivity.

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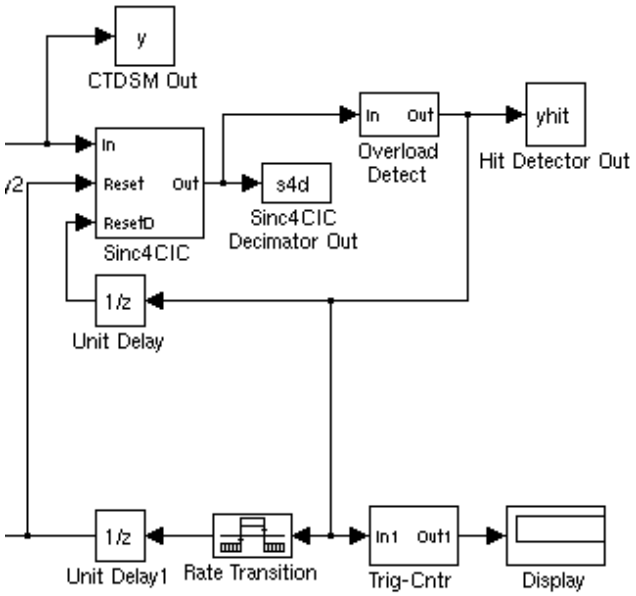
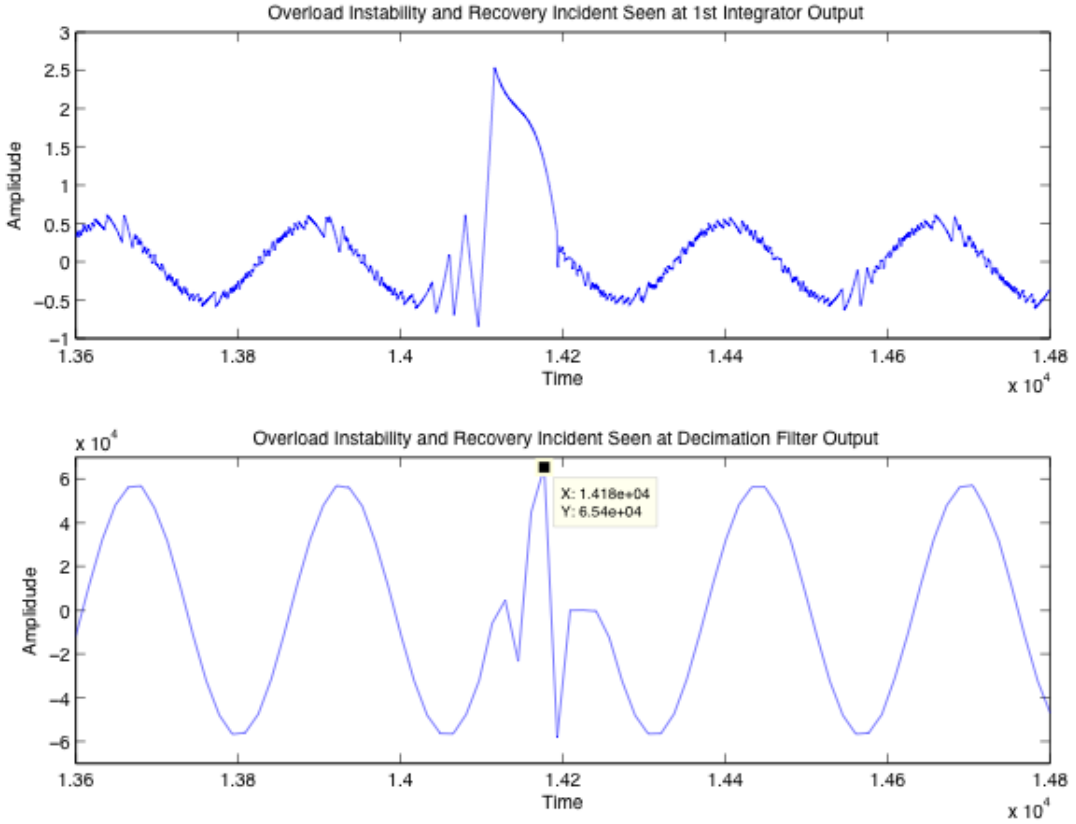
Stability Control (3)

Simulation Example of Detect / Reset Scheme:





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Multi-bit Quantizers in ΔΣ Modulators (1)

Why?:

- 'Linearly' solves the issue of stability by 'containing' the input and quantization error within the linear region of the quantizer.

For multi-bit modulators, the following theoretical result can be useful:

Consider a modulator with an M-step (i.e. $(M+1)$-level) quantizer which has one of the characteristics shown in Fig. 2.3 and 2.4. Let the initial input $y(0)$ to the quantizer be within its linear (no-overload) range. Then, the modulator is guaranteed not to experience overload for any input $u(n)$ such that $\max_n |u(n)| \le M + 2 - \|h\|_1$, where $\|h\|_1 = \sum_{n=0}^{\infty} |h(n)|$. Here, $h(n)$ is the inverse z-transform of the noise transfer function $H(z)$.

For example, if $M = 16$ and $H = (1 - z^{-1})^3$, then $\|h\|_1 = 8$ and thus any input with $\max_n |u(n)| < 10$ is guaranteed to not overload the modulator, i.e. this modulator system is stable for inputs up to 62.5% of the full-scale value 16.

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Multi-bit Quantizers in $\Delta\Sigma$ Modulators (2)

Benefits of Multi-bit:

- Use high-order loops with stable performance
- 6 dB improvement per bit for any order loop, assuming the DAC is perfectly linear and the loop is stable
- Reduce OSR or increase bandwidth of the converter
- Reduce DAC step-size, allowing slower integrators, improving slew rate limitations
- Tones reduced dramatically, so that dither is not required
- Low sensitivity to reference voltage noise for small inputs
- Reduces jitter sensitivity in continuous-time modulators

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Multi-bit Quantizers in $\Delta\Sigma$ Modulators (3)

Challenges associated with multi-bit:

- Any error in the DAC elements (e.g., mismatches in capacitors or resistors or current sources) produce a nonlinearity, which gets fed back to the input and therefore does not benefit from the noise shaping property.
- Traditional DAC error correction entails either hardware trimming or background calibration to minimize the error below the LSB of the converter. In most process technologies, capacitors cannot match better than 11 bits of accuracy.
- Requires DAC mismatch error correction for high resolution, which increases complexity of digital circuits, flash ADC, DAC switches, and layout.

DAC mismatch error correction can be accomplished by:

- DEM (Dynamic Element Matching) [3], pgs. 186-98
- Digitally-corrected with background calibration and RAM storage [3], p.202

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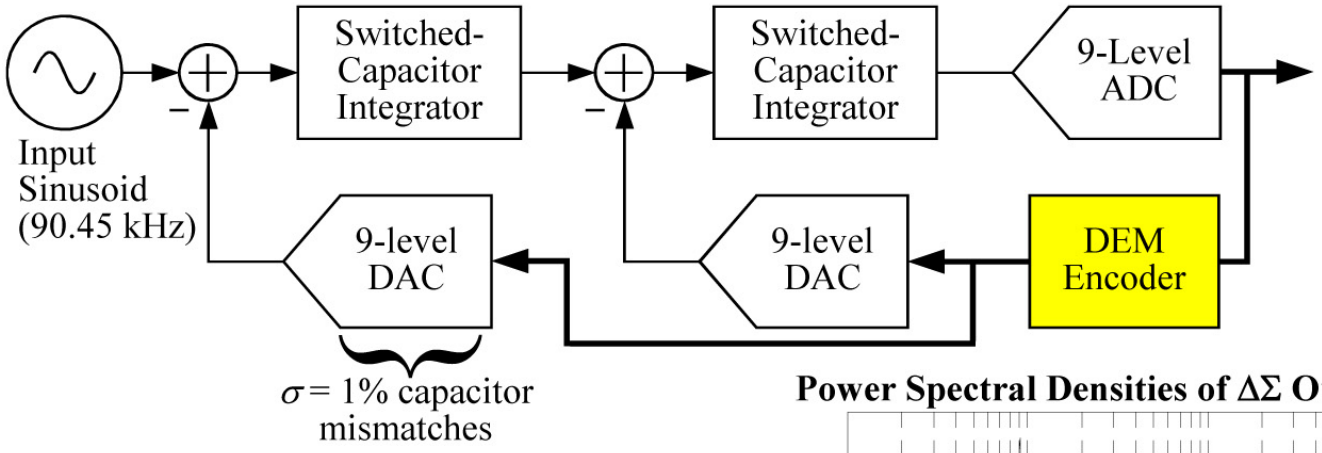
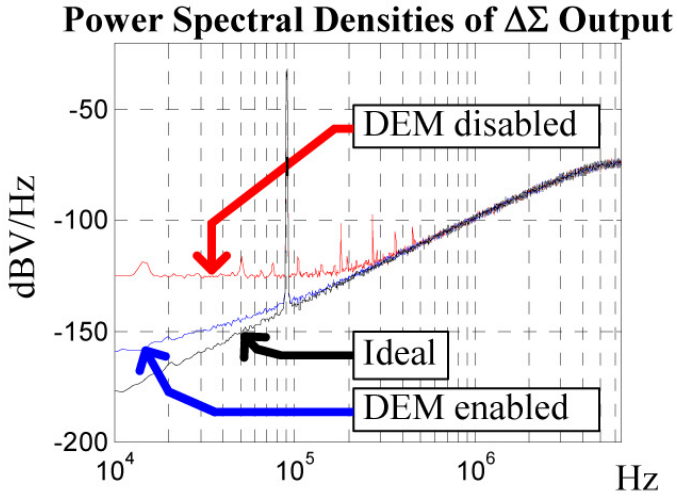
Mismatch Shaping DACs

Slide from Ian Galton [7]



Sample-rate = 13 MHz
Signal Band = 0 to 135 kHz
SNDR = 88.6 dB (ideal)
= 86.1 dB (1st-ord DEM)
= 73.0 dB (DEM disabled)



DEM ⇒ DAC noise has first-order highpass shape and is free of spurious tones (SNDR is only 2.5 dB less than ideal)

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DEM Techniques and Availability (1)

Cyclic Rotation, or "Data Weighted Averaging" (DWA)

- **Example**: A 3-bit (8-level) quantizer produces a code of….
  - Level #4 => DEM selects elements 1,2,3,4.
  - Level #2 => DEM selects elements 5,6.
  - Level #5 => DEM selects elements 7,8,1,2,3
  - Level #7 => DEM selects elements 4,5,6,7,8,1,2
  - The result is that we get a 1^{st}-order highpass shaping of the errors, which resembles the character of a 1^{st}-order 1-bit modulator, which causes tones and pattern noise in the spectra as it highpass filters the DAC errors.
- **Solutions**: whiten away the tones, but loose 6-9 dB over 'ideal'
  - Dithered DWA; Bi-directional DWA; ILA – Individual Level Averaging; Galton 'Tree' structure with dither
  - 2^{nd} -order differentiation (two-zeros at DC) transfer function shaping of the DEM falls short of ideal and only exaggerates noise near Fs/2. Also, the logic is more complex and not as straightforward as it would seem at first glance.

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DEM Techniques and Availability (2)

- That being said, practical implementations of 1st- and 2nd-order DEM's are in existence both in the literature and in products.
- DEM readily applicable to bandpass and quadrature architectures as well.
- Arbitrarily high orders have their practical limits. One cannot arbitrarily select any NTF for the DEM, because it has to be STABLE down to 1 bit at the internal quantizer of the DEM algorithm! Also, non-trivial NTF's may require a SORT algorithm that has to complete in one clock cycle of the oversampled clock interval.
- There are numerous DEM patents that one should be aware of before entering this technology. **Key patents include** (but not limited to)**:**
  - Motorola's basic concept patent for DWA or barrel shifting
  - Galton – 'Tree' Structure
  - Analog Devices – Butterfly Scrambler
  - Cirrus Logic's 2nd-order shaper
  - Broadcom's 2nd-order shaper
- Private DEM solutions are also available and can be licensed.

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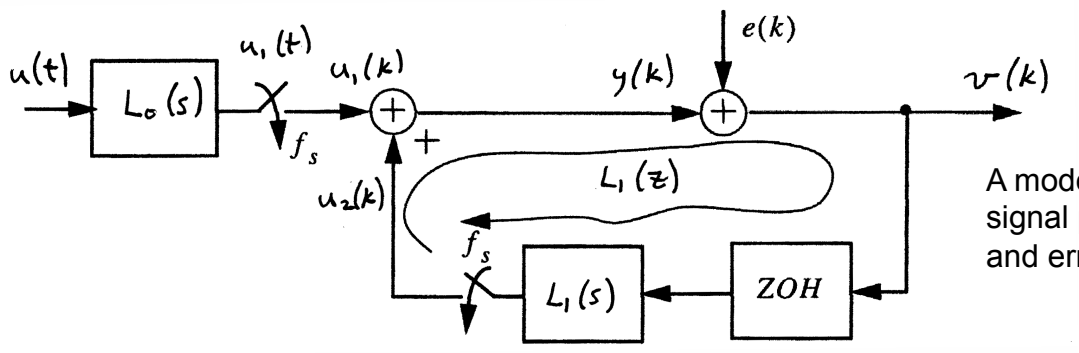
Continuous-Time ΔΣ Modulators (1)



A model abstraction of the effective signal processing operations of input and error filtering

The loop filters, $L_o(s)$ and $L_1(s)$, are in continuous time. A zero-order hold (ZOH) represents the DAC feedback pulse. The feedback is effectively a sampled-data system; therefore the NTF of the system can be expressed in the *z*-domain. Since the Laplace transform of a ZOH function is known, given by $(1 - e^{-s} / s)$, we can apply the z-transform to the cascaded combination of the ZOH and the feedback filter and derive $L_1(z)$.

The STF for the continuous-time modulator is the convolution of the continuous-time input filter, $L_o(s)$, with the effective discrete-time NTF, $L_1(z)$

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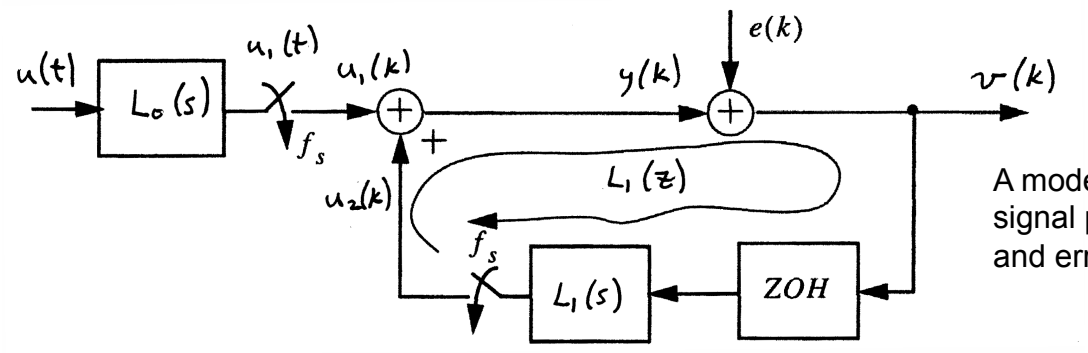
Continuous-Time ΔΣ Modulators (2)



A model abstraction of the effective signal processing operations of input and error filtering

$$L_1(z) = Z\left[\frac{1-e^{-s}}{s} L_1(s)\right]$$

$$STF = \frac{L_0(s)}{1-L_1(z)} = L_0(s) \cdot NTF(z)$$

$$STF(j\omega) = \frac{L_0(j\omega)}{1-L_1(e^{j\omega})} = L_0(j\omega) \cdot NTF(e^{j\omega})$$

Example: substitute NTF with a 2nd-order modulator NTF

$$STF = \left(\frac{\left(1-z^{-1}\right)}{s}\right)^2$$

Evaluating in frequency domain gives a *sinc-squared* filter expression

$$STF(f) = \left(\frac{\sin(\pi f)}{\pi f}\right)^2$$

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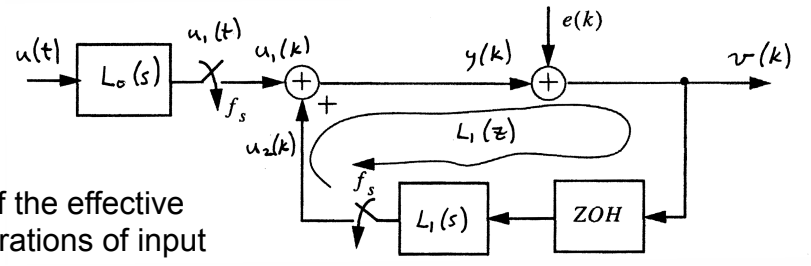
Continuous-Time ΔΣ Modulators (3)



A model abstraction of the effective signal processing operations of input and error filtering

Example: 2nd-order modulator NTF

$$STF(f) = \left(\frac{\sin(\pi f)}{\pi f}\right)^2$$

Thus, a continuous-time modulator of order M, having all of its NTF zeros at $z=1$, has an inherent M-order $sinc$ pre-filter or anti-alias filter, placing deep notches around multiples of the sampling frequency. When the modulator has a more complicated filter structure, such as when the NTF zeros are not exclusively at $z=1$ but optimally spread, then the pre-filter is no longer a pure $sinc^M$ function, but may retain the desirable $sinc^M$ characteristic of nulls around multiples of the sampling frequency.

Therefore, the STF of a continuous-time modulator has a unique property: it possesses inherent anti-aliasing.

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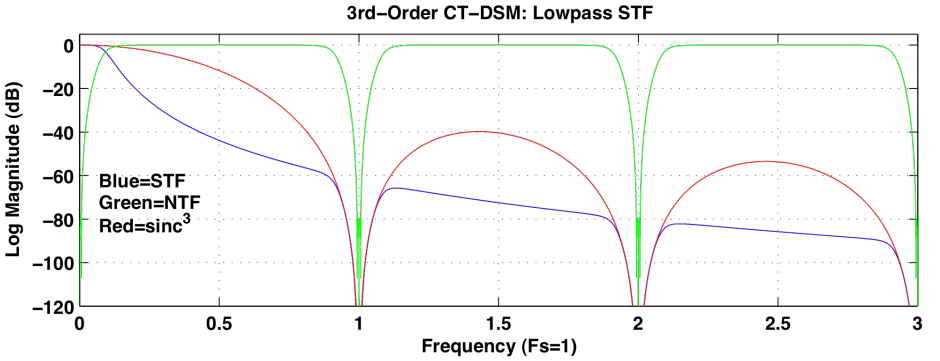
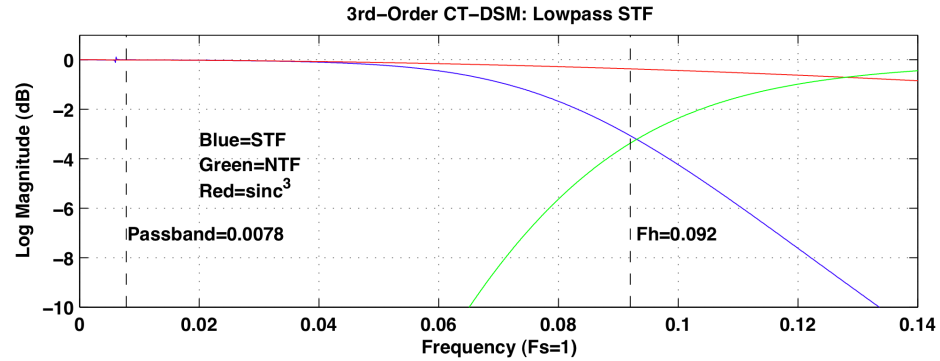
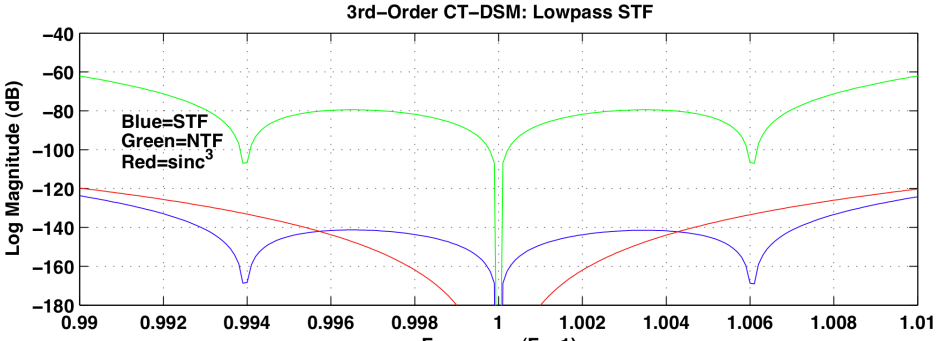
Continuous-Time ΔΣ Modulators (4)







The STF of a CTDSM is multiplication of $Lo_c(s)$ (the continuous-time transfer function from input to quantizer) with the discrete-time noise transfer function $NTF(z)$

$STF(j\omega) = Lo_c(j\omega)\ NTF(e^{j\omega})$

The NTF is essentially a highpass filter with a cutoff freq f_h near $F_s/10$. The STF poles are the same as for the NTF, so if the STF has no zeros, it will look like a lowpass version of the same filter in low frequency, and a sinc^M (an M-order DSM) at multiples of F_s

These principles combine to give a desirable STF.

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Excess loop delay in CTΔΣM

- Beginning at the clock edge of the flash A/D converter and propagating through the DAC feedback path into the integrators.
  - Quantizer metastability: This delay is not fixed, rather, it is variable, and is a function of the differential input voltage of the comparators.
  - If the DAC pulse goes past *T=1*, the order of the ΔΣ modulator actually increases by one, (*m+1*), and the system is not controllable by an *m*-order set of coefficients [Cherry 1999].
  - Any excess delay causes peaking in the NTF, increasing the dynamic range requirements, often requiring a multi-bit DAC to keep the system stable.
  - Newer solutions: deliberately adding digital delay with multiple half-latches in series. This causes the probability of a decision error to decrease favorably. Goal is one-half clock delay $(T_s / 2)$ around the quantizer and one period delay in the outer loops.
  - Still, must solve modeling and synthesis problem. It is no longer a classic delta-sigma structure
  - Pulse response around the loop: must take into account delays of the op-amps and other parasitic elements, and must be modeled. Can use modeling and optimization to compensate and match a given desired pulse response.

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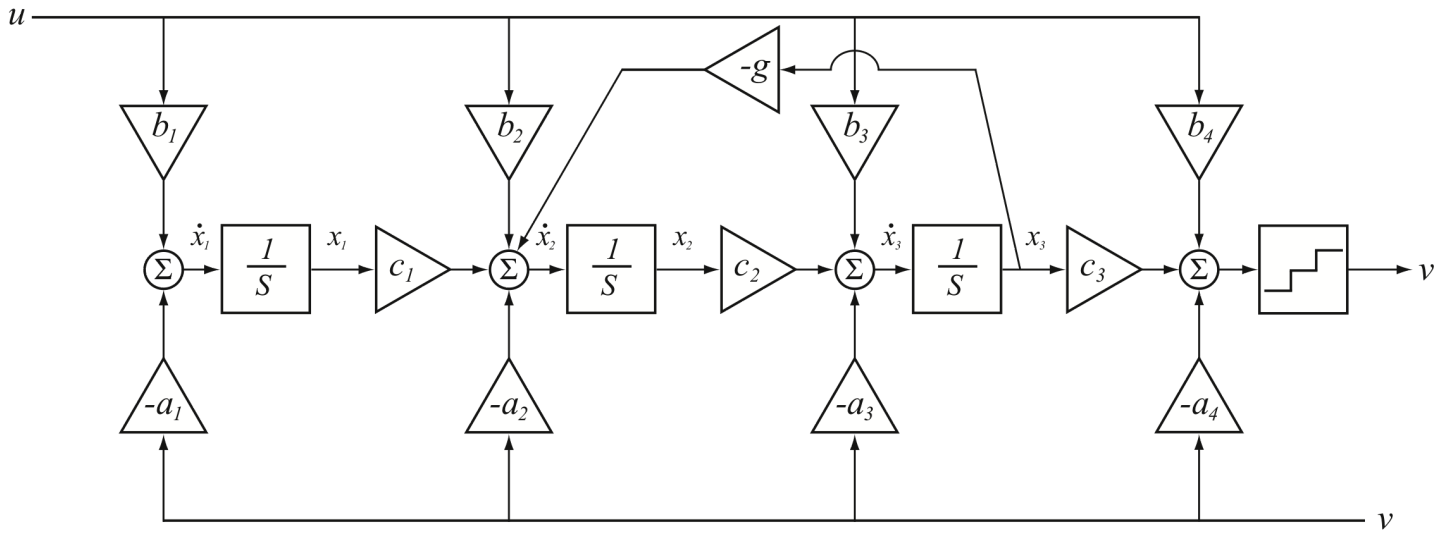
3rd-Order CTΔΣM in State-Space: Ideal SISO Zero-Delay Model



ABCD State-Space Equations:

$$\dot{x} = \begin{bmatrix} 0 & 0 & 0 \\ c_1 & 0 & -g \\ 0 & c_2 & 0 \end{bmatrix} x + \begin{bmatrix} b_1 & -a_1 \\ b_2 & -a_2 \\ b_3 & -a_3 \end{bmatrix} \begin{bmatrix} u \\ v \end{bmatrix}$$

$$y = \begin{bmatrix} 0 & 0 & c_3 \end{bmatrix} x + \begin{bmatrix} b_4 & -a_4 \end{bmatrix} \begin{bmatrix} u \\ v \end{bmatrix}$$

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CTΔΣM : Least-Squares Solution

- Cannot have zero delay from the quantizer.
- Build a MIMO system of order *m+1* ($a_{m+1} \neq 0$).
- Place a known amount of digital delay ($nT_s/2$) on each feedback input.
- Target the pulse response of an ideal DTΔΣM SISO system of order *m.*
- Solve for $a_1 \ldots a_{m+1}$ by Least Squares.
- Ensure that at the discrete sampling instances, nT_s, we produce the same output at the quantizer from the CT system as from the target DT system.

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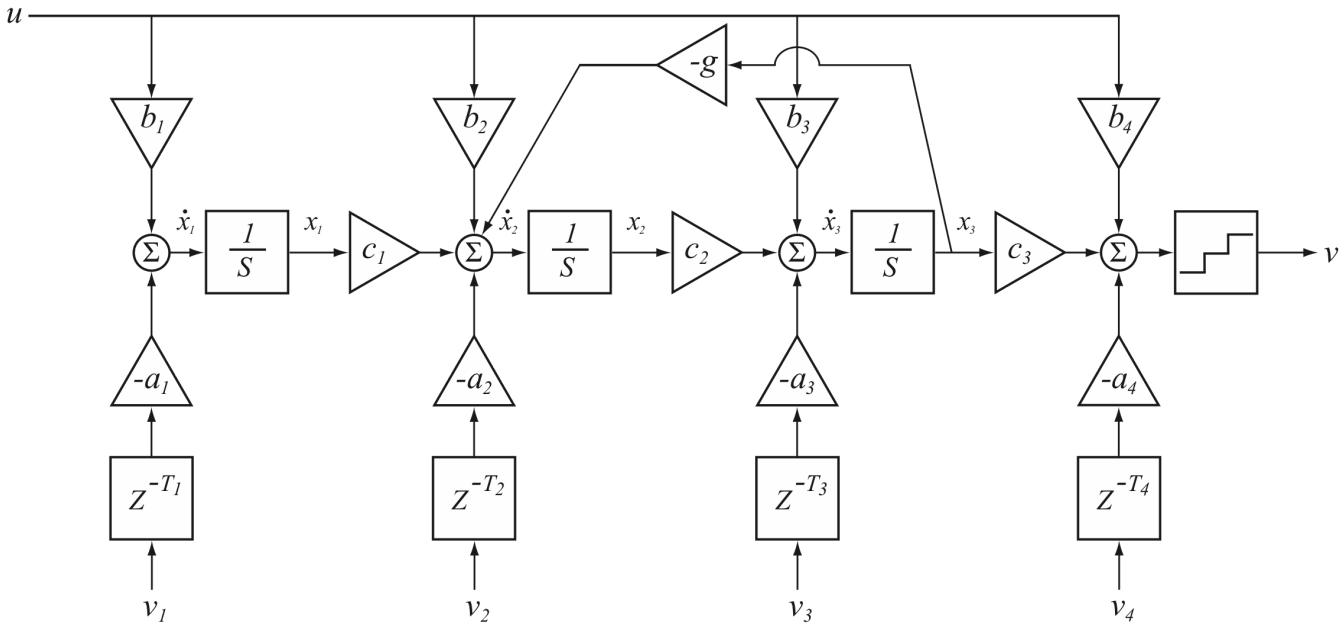
3rd-Order CTΔΣM in State-Space: MIMO Model With Delays



ABCD State-Space Equations:

$$\dot{x} = \begin{bmatrix} 0 & 0 & 0 \\ c_1 & 0 & -g \\ 0 & c_2 & 0 \end{bmatrix} x + \begin{bmatrix} -a_1 \\ -a_2 \\ -a_3 \end{bmatrix} v$$

$$y = \begin{bmatrix} 0 & 0 & c_3 \end{bmatrix} x - a_4 v_4$$

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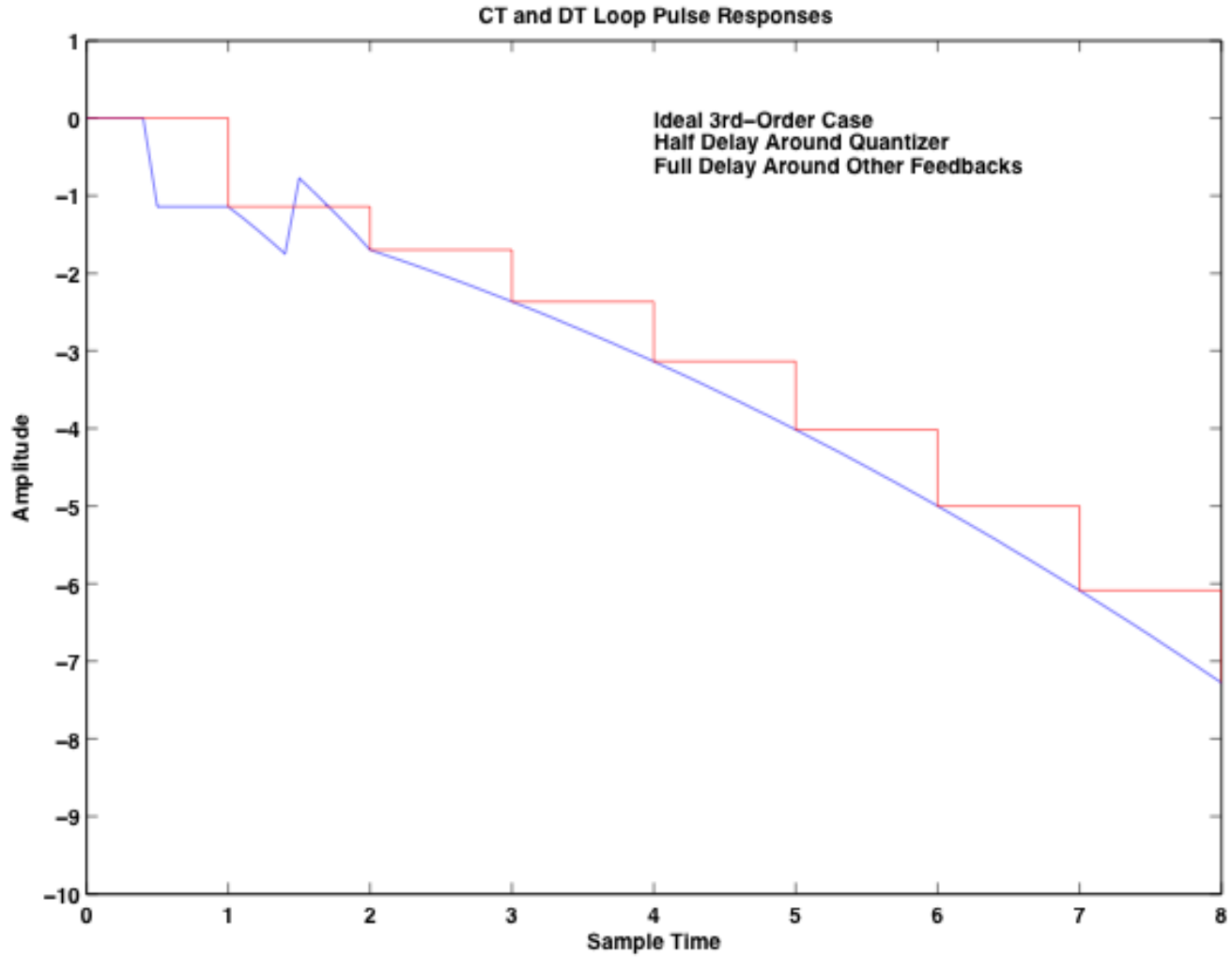
3rd-Order CTΔΣM and DTΔΣM: Pulse Responses from Synthesis



Loop Delays:
T/2 for a_4
T for a_3, a_2, a_1

Ideal Op-Amps

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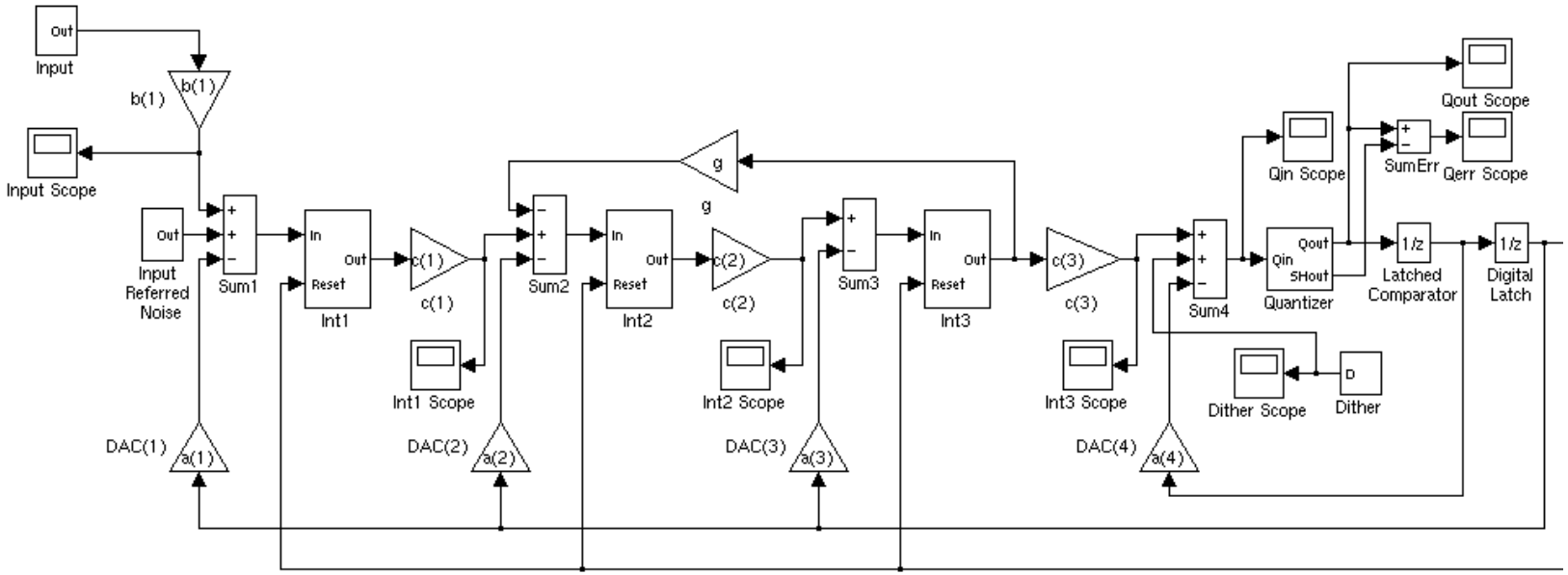
Simulink Model of CTΔΣM



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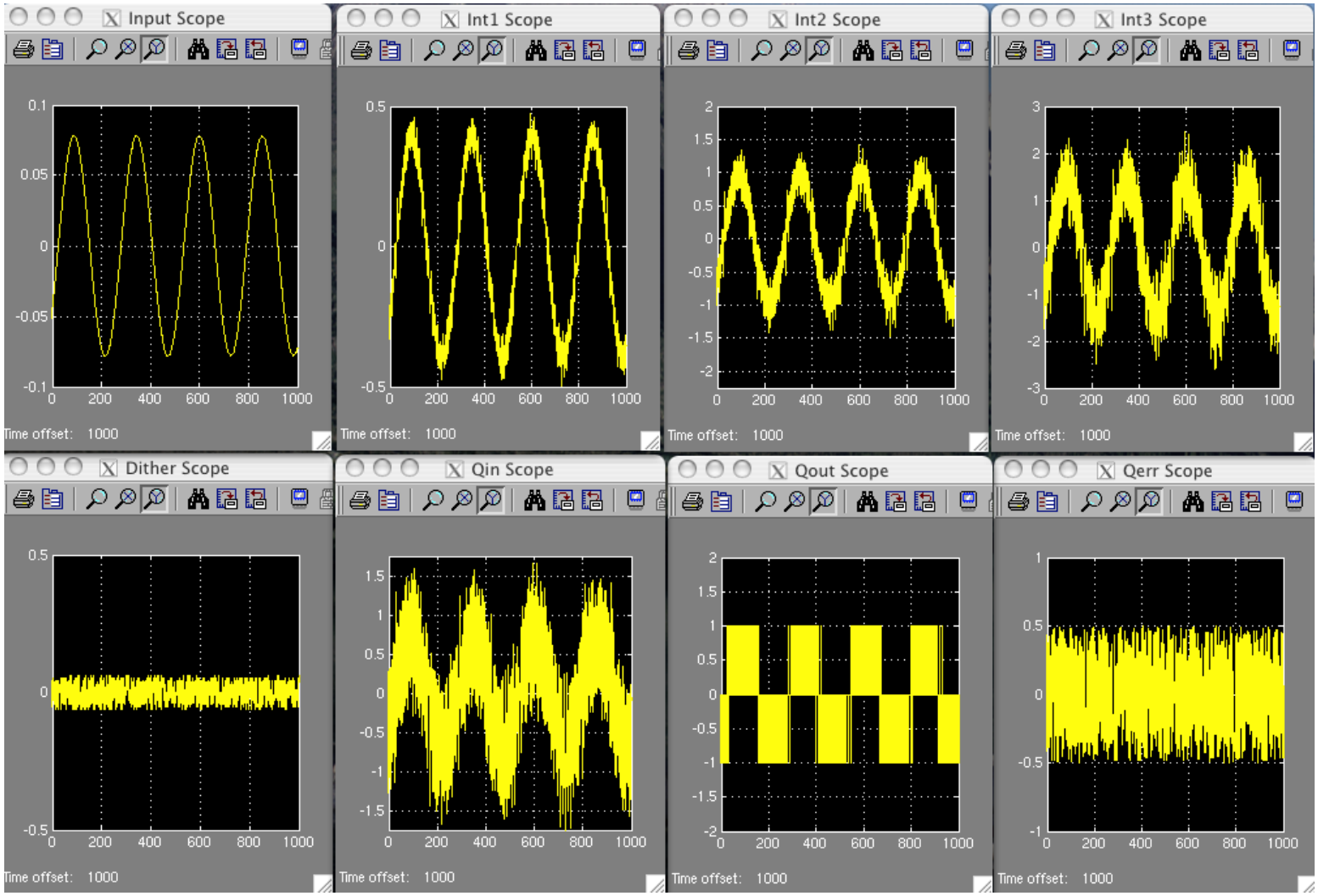
Simulation Scopes of CTΔΣM



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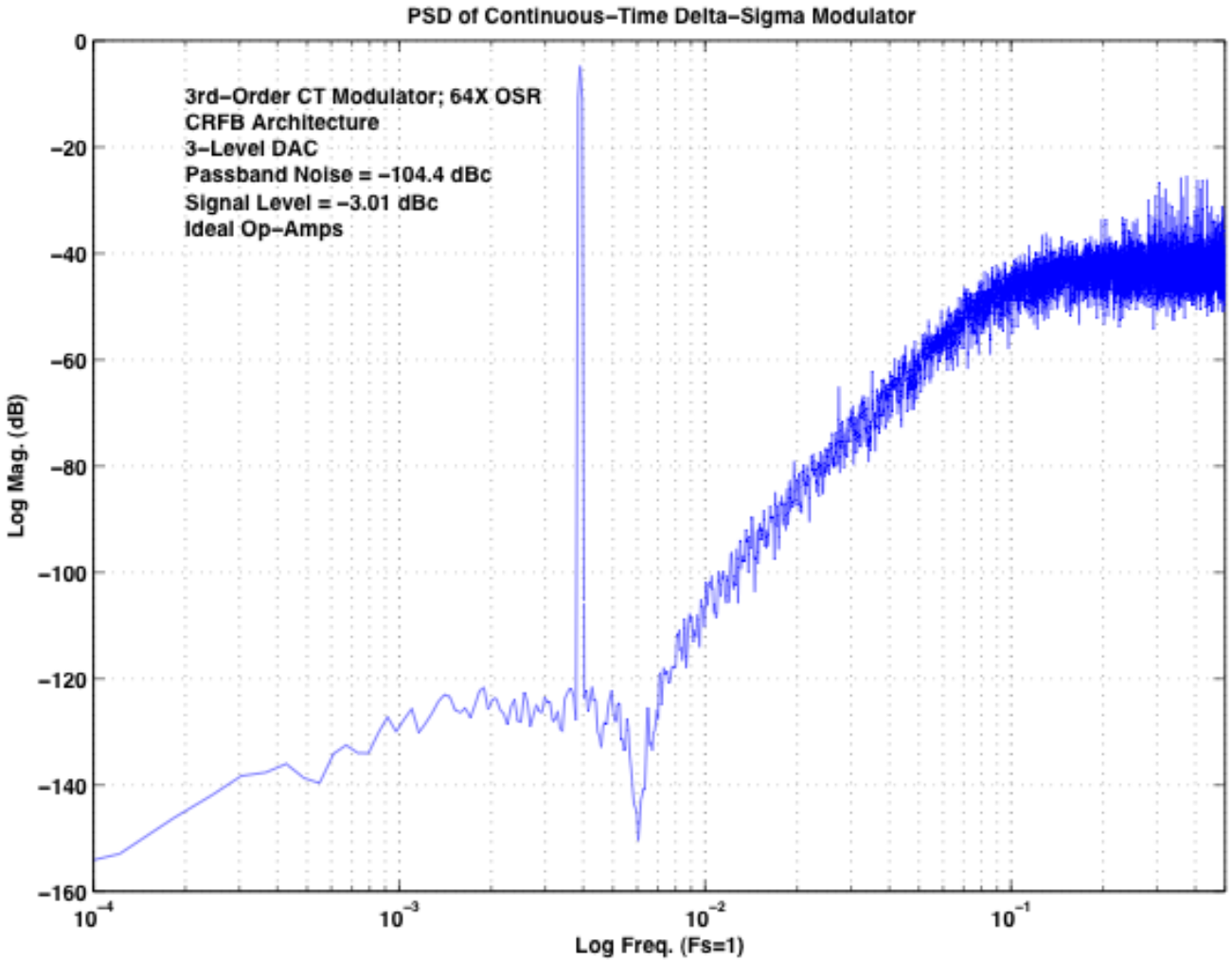
PSD of CTΔΣM



Loop Delays:
T/2 for a_4
T for a_3, a_2, a_1

Ideal Op-Amps

PSD identical to DT case (not shown)

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Finite Gains; Process Variations

- Can expand the MIMO state-space model with a more complicated Op-Amp model
- As for RC time constants with process variation, when the gains increase, the SQNR holds up until the loop eventually goes unstable (20% per block increase will start instability).
- Can create a set of 'a' coefficients that gives ideal performance even at the extremes of process corners for all the elements that can vary, and then self-calibrate the chip and select the corresponding set of 'a' coefficients stored in memory which optimize performance.

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Jitter (1)

- There are two fundamental types of jitter to consider [Risbo 1994]:
  - Current-integrating DAC: The hold time will be modulated by the jitter sequence, since the output signal only changes state at the sampling instants. The in-band SNR for R-times oversampled sinusoidal output with amplitude A and RMS jitter t_{rms} is:

$$\mathrm{SNR_{NRZ}} = 10\log\frac{R\ A^2/2}{2.7\left(\frac{t_{\mathrm{RMS}}}{T}\right)^2}\ \mathrm{dB}$$

  - Switched-Cap. DAC: This is far less sensitive to jitter since the pulse waveform is the result of a capacitor charge or discharge that is independent of the sampling time instants. The in-band jitter noise power can be calculated by integrating the noise power density assuming the error sequence is white with t^2_{rms} variance:

$$\mathrm{SNR_{pulse}} = 10\log\frac{3\ R^3\ A^2/2}{\pi^2\left(\frac{t_{\mathrm{RMS}}}{T}\right)^2}\ \mathrm{dB}$$

    - Example: R = 64; A = 1; Fs = 256 MHz; SNR = 90 dB; Pulse-type DT feedback
    - Formula for Pulse-type: t_{rms}= 25 ps
    - Simulink model and simulation for Pulse-type: t_{rms}= 35 ps
    - State-of-the art is below 1 ps, so we are not fundamentally limited, however,…
    - If we use CT feedback instead, t_{rms}= 0.4 ps

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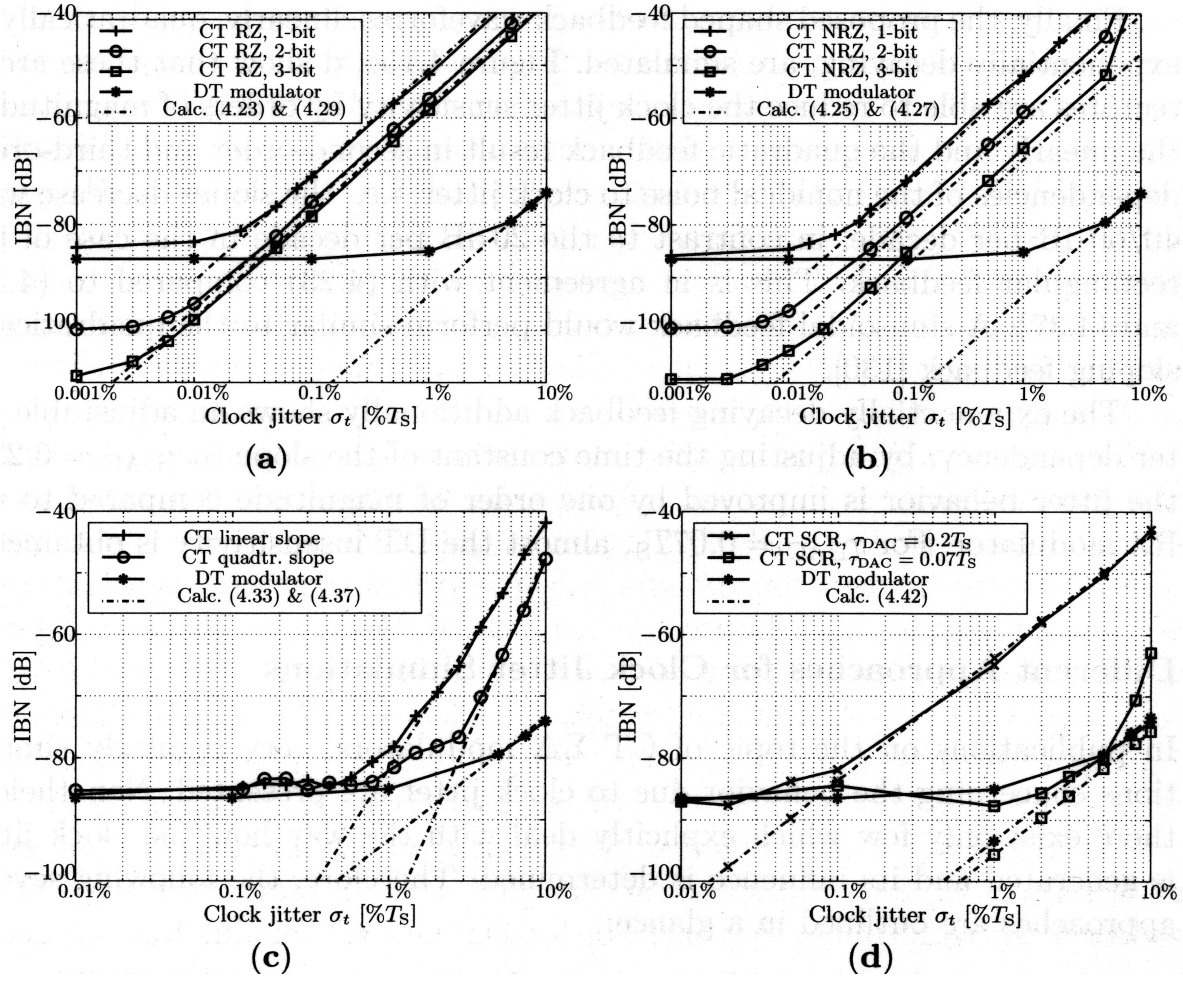
Jitter (2)

Ortmanns [Ref]: Jitter in CTDSM can be drastically reduced with pulse shaping circuits.



Ortmanns [Ref]:

From Best to Worst:

Example: IBN Req. = -80 dB

DT=> 4%

CT SCR 0.07Ts => 4%

CT quad. => 2%

CT NRZ 3-bit => 0.2%

CT SCR 0.2Ts => 0.15%

CT RZ 3-bit => 0.08%

CT NRZ 2-bit => 0.09%

CT RZ 2-bit => 0.06%

CT NRZ 1-bit => 0.03%

CT RZ 1-bit => 0.02%

Assume Fs = 160 MHz

Ts = 6.25 ns

4% Ts = 250 ps

2% Ts = 125 ps

0.2% Ts = 12.5 ps

0.08% Ts = 5 ps

0.02% Ts = 1.25 ps

Ratio: Best/Worst = 200X

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Pipeline or CTΔΣM ?

Slide from Jorge Grilo [8]

- CTΔΣM
  - Requires process tuning and control of clock performance
  - Excellent for SOC solutions as post filtering requirements are likely to be exceeded by channel-selection filters
    - ADC current consumption becomes modulator consumption
    - Stand-alone implementations require dedicated digital filter and possibly integrated low jitter PLL
      - 20 MHz bandwidth, 12-ENOB requires sub 1-ps-rms wideband jitter
  - Excellent for multi-channel products – Less substrate noise
  - CT input greatly simplifies interface requirements
  - Intrinsic anti-aliasing properties
  - For low current with ENOB > 11 over 10-20 MHz, external reference decoupling is necessary
  - Moderate to high OSR: > 8
  - Commercially viable (ADI, National, others in SOC's)

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Pipeline or CTΔΣM ? (2)

Slide from Jorge Grilo [8]

- Silicon Example #1 - CTΔΣM
  - Signal bandwidth: 10 MHz
  - 11 ENOB
  - 320 MSPS
  - 65 nm CMOS process, 1.2V supply
  - Second-order loop (CTDS) with multibit quantizer
    - Does not utilize DEM
  - Integrated references and bandgap
  - SOC
  - 9 mA / channel (modulator) or 11 mW

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Pipeline or CTΔΣM ? (3)

Slide from Jorge Grilo [8]

- Silicon Example #2 - CTΔΣM
  - Signal bandwidth: 4 MHz
  - 12 ENOB
  - 200 MSPS
  - 130 nm CMOS process, 1.2V supply
  - Fifth-order loop (CTDS) with multibit quantizer
    - Utilizes DEM
  - SOC
  - 6.5 mA / channel (modulator) or 8 mW
    - Does not include reference / bandgap

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Pipeline or CTΔΣM ? (4)

Slide from Jorge Grilo [8]

- Pipeline
  - Calibration required for ENOB > 10-11 bits
  - Excellent for SOC and stand-alone solutions alike with moderate OSR (<8)
    - Up to full Nyquist bandwidth
  - No digital filtering required – full-rate output
  - Well established design techniques
    - Some novel calibration work published over recent years may further advance use of pipeline ADC's

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Pipeline or CTΔΣM ? (5)

Slide from Jorge Grilo [8]

- Silicon Example #1 - Pipeline
  - Signal bandwidth: 4 MHz
  - 10 ENOB
  - 40 MSPS
  - 130 nm CMOS process, 1.2V supply
  - No calibration
  - Switched-capacitor
  - SOC
  - Integrated references and bandgap
  - 12 mA / channel or 15 mW
    - Excludes references

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Pipeline or CTΔΣM ? (6)

Slide from Jorge Grilo [8]

- Silicon Example #2 - Pipeline
  - Signal bandwidth: 50 MHz
  - 12 ENOB
  - 100 MSPS
  - 90 nm CMOS process, 1.2V supply
  - Miscellaneous calibration techniques
  - Switched-capacitor
  - Stand-alone
  - References with external decoupling
  - 100 mA / channel or 120 mW

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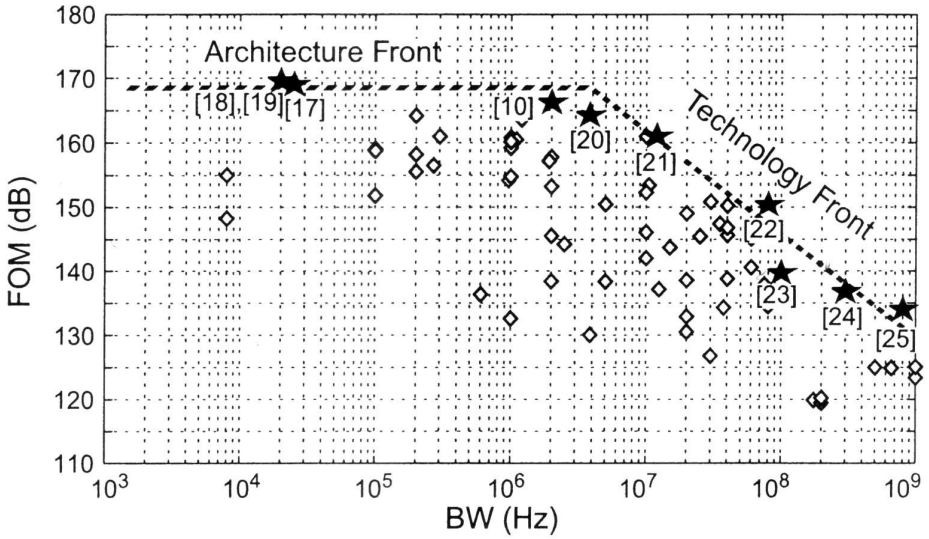
FOM vs. DR, BW, P

- FOM formulas in the literature are based on the trade-offs between bandwidth, power consumption, and dynamic range: FOM = DR_{dB} + 10 log(BW / P)
- For a constant FOM, doubling the BW with a constant DR requires a doubling of power. Similarly, a 3dB increase in DR requires a doubling of power for the same BW. Therefore, DR and BW can be traded off 3dB/octave.
- FOM's only modestly improving with technology shrinkage.
- The faster the sampling clock, the worse the FOM.
- Single-bit delta-sigma has very poor 'coding efficiency,' as too much power is wasted out of band.
- For delta-sigma converters, FOM improves with multi-bit and lower sampling clock. FOM further improves by absorbing the anti-alias filter functions that are implicit in the design, and the future FOM can be better than a comparable pipeline converter.



FOM vs. bandwidth for published ADCs.

Architecture	BW	DR (dB)	P (mW)	FOM
ΔΣ: 5(4b) SC [18]	20 kHz	111	27.5	170
ΔΣ: 3(1b) SC [19]	20 kHz	88	0.14	170
ΔΣ: 2(1b)-1(1b) SC [17]	25 kHz	99	2.5	169
ΔΣ: 2(5b)-2(3b)-1(3b) [10]	2 MHz	95	150	166
ΔΣ: 5(1b) gm-C [20]	3.8 MHz	78	9	164
ΔΣ: 3(6b) gm-C [21]	12 MHz	79	75	161
Pipeline [22]	80 MHz	66	290	150
Pipeline [23]	100 MHz	51	135	140
Folding [24]	300 MHz	45	200	137
Folding [25]	800 MHz	46	1270	134

Published ADCs achieving the highest FOM at a given BW.

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FOM vs. DR, BW, P

- Examples:
  - NXP (Philips): ISSCC '07, Paper 13.1
    - SNR = 71 dB; BW = 20 MHz; P = 56 mW => FOM(dB) = 156 dB = 0.2 pJ / Conv.
    - Chip area = 0.5 mm^2; 90-nm CMOS; 1.2V;
    - Complex IF CTDSM
  - NXP (Philips): ISSCC '07, Paper 13.3
    - BW: Covers 2 decades (0.1 MHz - 10 MHz) in 121 steps of bandwidth => GSM through WiMAX
    - SNR: { 52 - 85 } dB; P = { 1.4 - 7 } mW; FOM: { 0.2 - 0.8 } pJ / Conv.
    - Chip area = ? ; 90-nm CMOS; 1.2V; CTDSM, 5th-Order, 1-bit
  - Infineon: ISSCC '05, Paper 27.1
    - SNR: 74 dB; BW = 2 MHz; P = 3 mW; FOM(dB): 162
    - Chip area = 0.3 mm^2; 130-nm CMOS; 1.5V
    - CTDSM, 3rd-Order, 4-bit, Fs = 104 MHz => OSR = 52
    - Uses 3 comparators (tracking ADC) instead of flash with 15 comparators
  - Philips: JSSC '04, Vol. 39, No. 12, Dec. 2004, pp. 2152-60
    - (An older and less efficient design)
    - SNR = 68 dB; BW = 20 MHz (I + Q); P = 122 mW ==> FOM(dB) = 150
    - 2-2 Cascaded CTDSM & 4-bit quantizers; Chip Area: 1.7 mm^2

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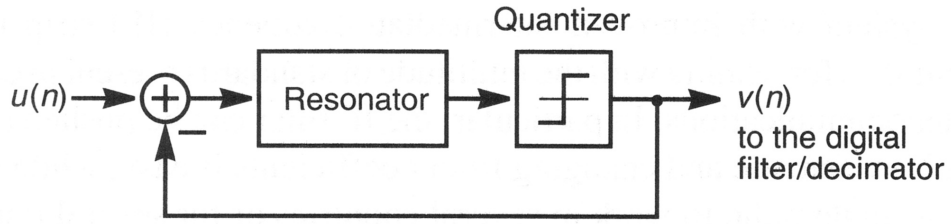
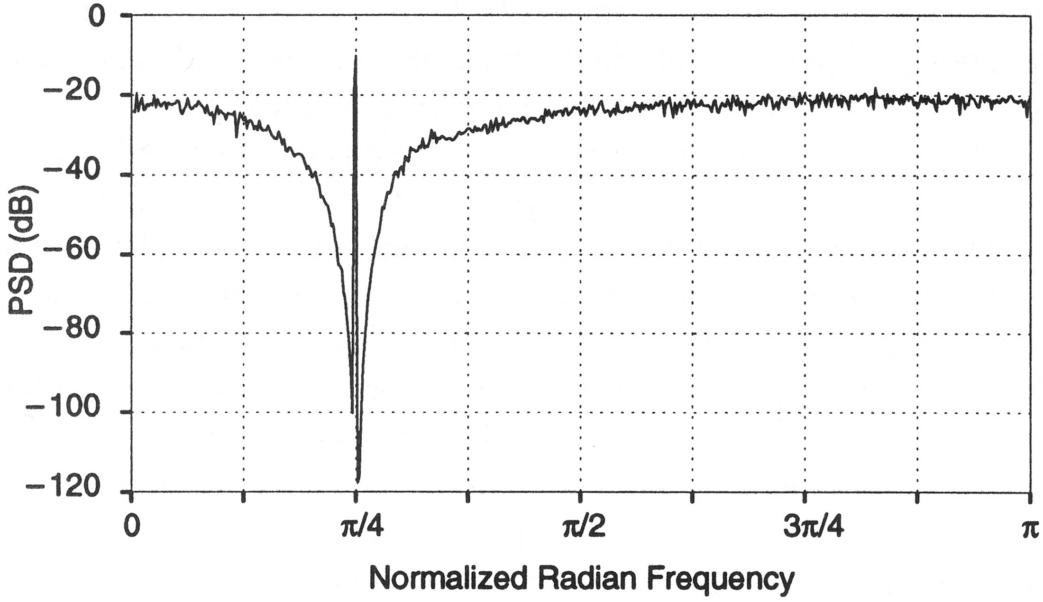
Bandpass $\Delta\Sigma$ Modulators (1)

- Research started in 1980's, and continues to be heavily researched.
- Rather than shaping the quantization error near zero frequency (baseband), the loop filter can be centered at any intermediate frequency (IF). This allows for 'complex' bandpass sampling.



A bandpass noise-shaping feedback loop.



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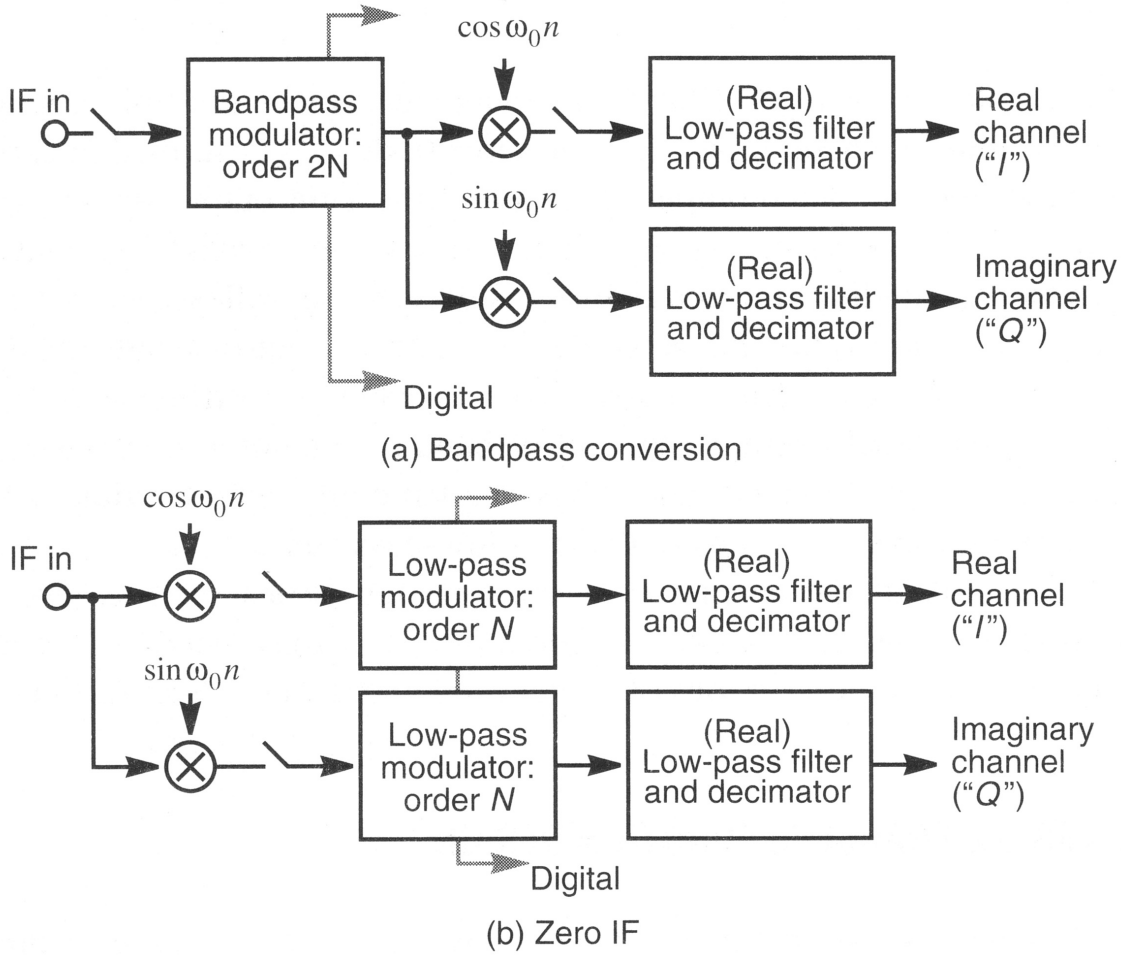
Bandpass ΔΣ Modulators (2)

- Bandpass ΔΣ A/D converter replacing conventional Zero IF quadrature analog down conversion mixer and separate I / Q analog signal paths.
- The I / Q mixer is now digital rather than analog



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Bandpass $\Delta\Sigma$ Modulators (3)

Advantages:

- The I / Q mixer is digital, and has no mismatches between channels.
- Theoretically, higher resolution in the signal band of interest.

Disadvantages:

- High frequency analog circuits required for the loop filters, prone to high noise, high power consumption; slew rates must be sufficiently fast to keep up with the clock rates.
- The resonator design must be high Q in order to achieve high resolution in the signal band of interest.
- The resonator center frequency must be accurately placed, or else it must go through a tuning and calibration cycle.
- Requires special technologies outside the realm of standard CMOS.

Conclusion:

- To date, limited commercial success, due to high power, high cost.
- Great future potential as IC technologies keep improving.

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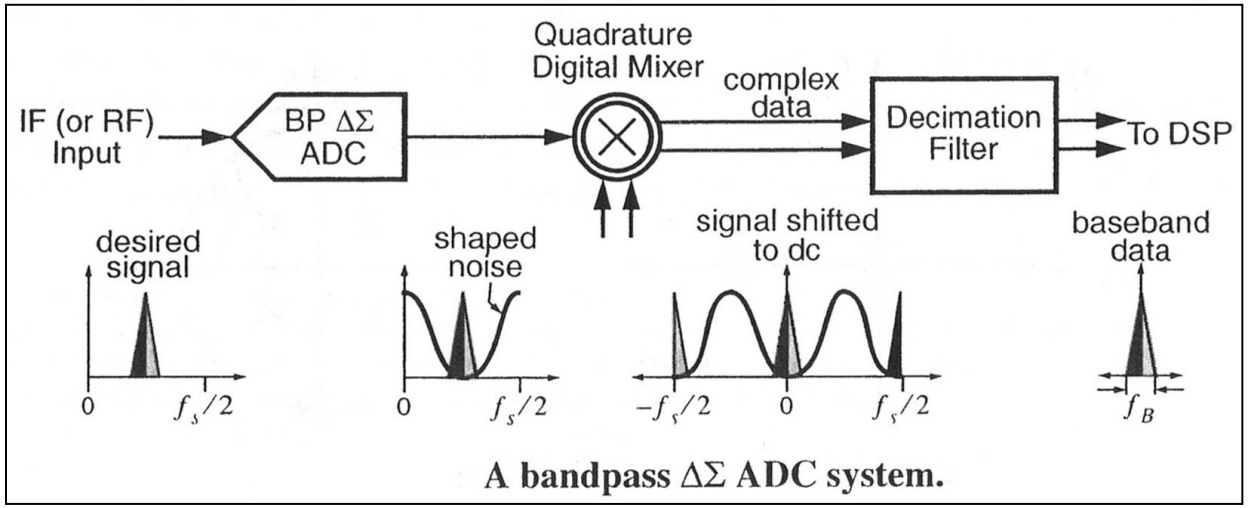
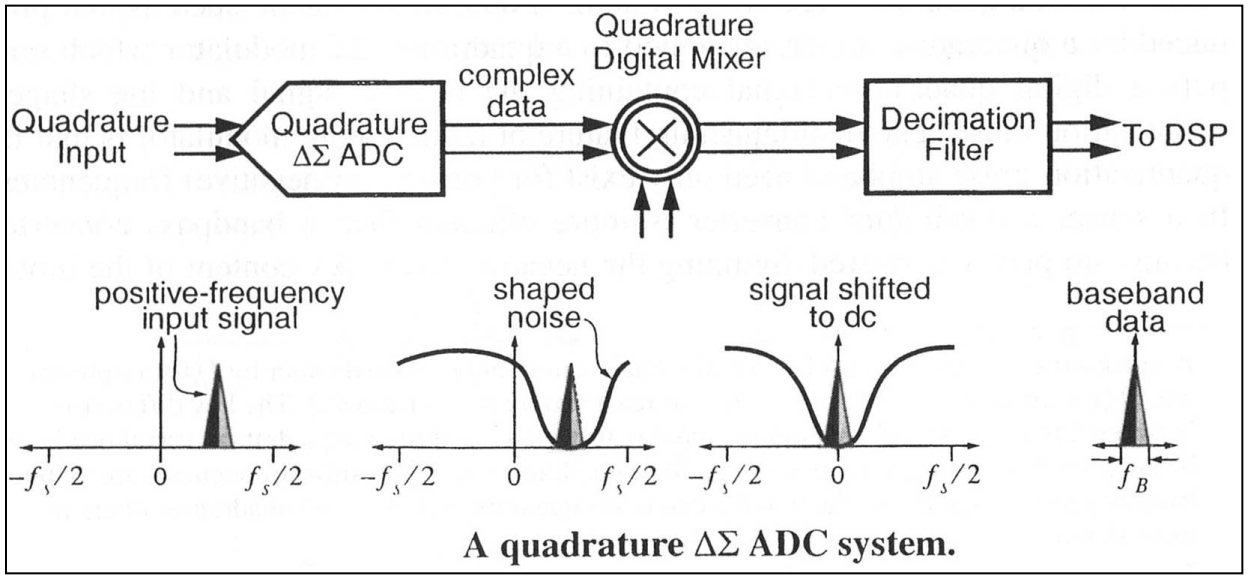
Quadrature ΔΣ Modulators (1)



A bandpass ΔΣ ADC system.



A quadrature ΔΣ ADC system.

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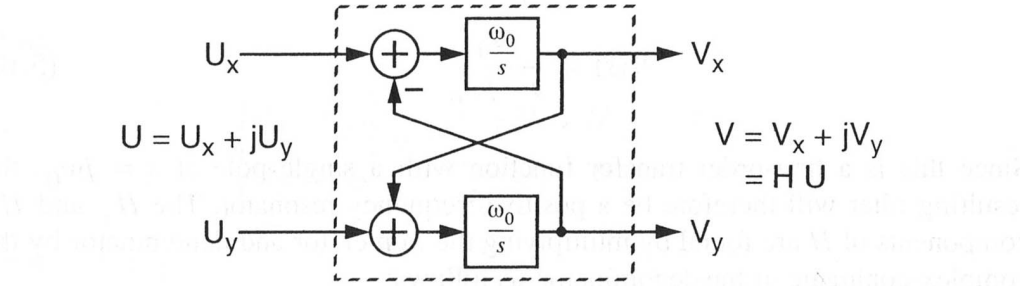
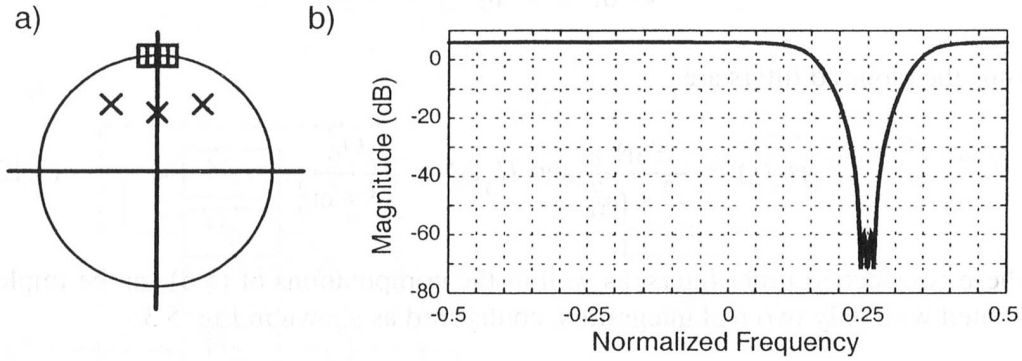
Quadrature ΔΣ Modulators (2)



A quadrature resonator, $H(s) = \omega_0/(s - j\omega_0)$.



a) Pole-zero and b) magnitude plots for a quadrature NTF with *OSR* = 32.

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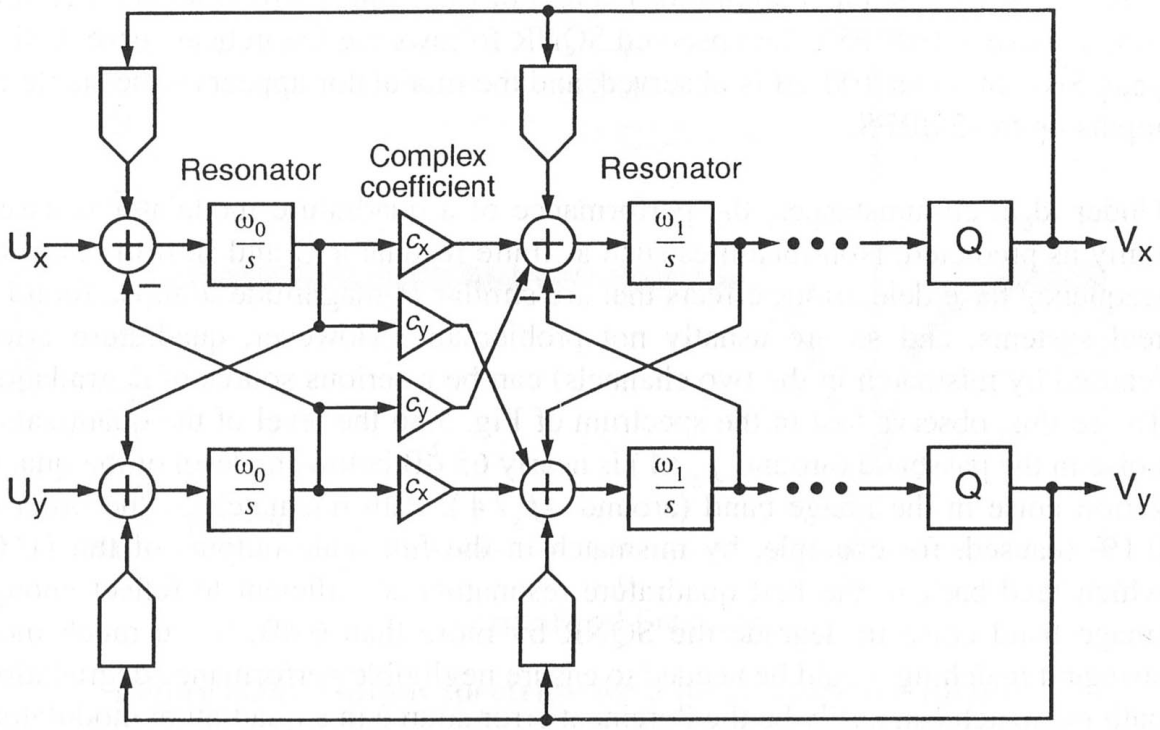
Quadrature $\Delta\Sigma$ Modulators (3)



A quadrature modulator employing the feedback topology.

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Quadrature $\Delta\Sigma$ Modulators (4)

Quadrature Advantages over a Bandpass System:

- Exploits the advantages of having a quadrature mixer at the front end: image rejection and double the bandwidth compared with a real-only system.
- It doubles the bandwidth without doubling the hardware or clock frequency.

Disadvantages:

- Mismatch between the two sides of the architecture create images that are not infinitely rejected. High image rejection requires high amplitude and phase accuracy.
- However, mismatch effects can be reduced by exploiting DSP adaptive mismatch cancellation.

Conclusion:

- An extension beyond bandpass modulators, with great future promise and better exploitation of DSP, but no commercial success yet.

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RF_2Bits and $Bits_2RF$

The Ultimate Dream:

- To couple the digital baseband directly to RF with the least analog hardware. It's easier said than done. "If we dream, we progress!"

The Ultimate Challenges:

- Cost, size, power efficiency, dynamic range, spectral purity, flexibility.

Is there anything conceptually beyond Bandpass or Quadrature Delta-Sigma? Yes!

- Some patents and papers pointing to new directions.
- Classes of transmitters that make the problems more digital, but perhaps the silicon technology has not caught up with these new architectures.
- Shape out-of-band quantization noise digitally at RF frequencies rather than at IF or baseband frequencies; enables the placement of digital spectral nulls in selected bands of the broader spectrum.
- Class-C, -D, -E PA's that replace a classical PA by using a power DAC to drive a high-Q resonator, which stores and delivers power to the antenna or load.
- All-digital PLL, such as TI's approach.

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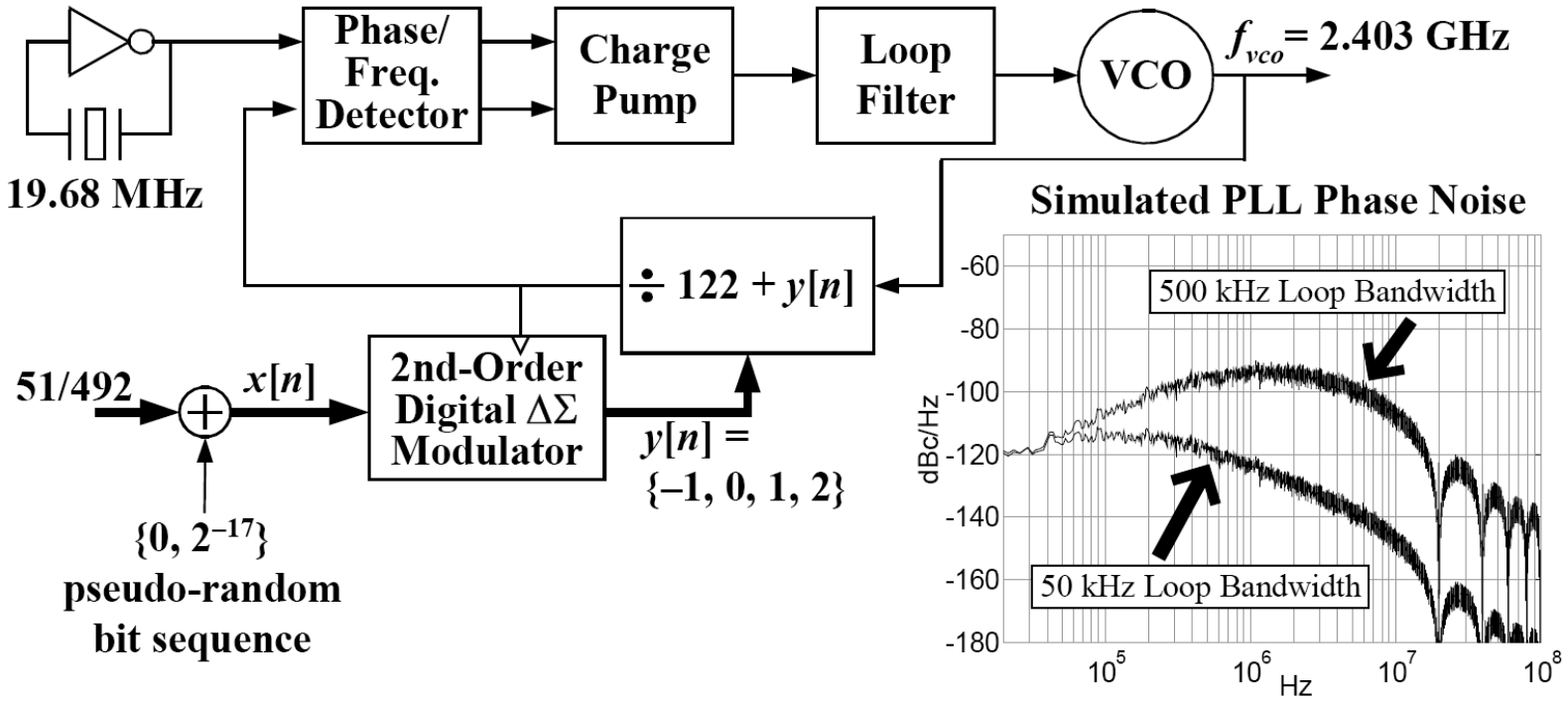
Fractional-N PLL's

Slide from Ian Galton [7]

Today, most fractional-N phaselock loop frequency synthesizers employ a digital delta-sigma noise shaper to randomize the spurious frequencies normally generated.



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Applications: Audio

Voice and Audio were the first two commercial applications of delta-sigma conversion, beginning in the late '80s and early 90's, and continue to dominate the converter space in these fields.

Now every CD player, MP3 player, DVD player, digital TV set, using $\Delta\Sigma M$.

Advantages:

•16- 20-bit ENOB can be achieved at low cost.

•Integrated as SOC along with many other functions for PC's, cell phones, portable audio players.

Major Suppliers:

Cirrus (Crystal); Wolfsen; Mediatek; Realtek; Sigmatel; ADI;

Architecture:

•Cirrus, Wolfsen, ADI all using multi-bit DEM, as it provides the best linearity, lowest power, highest resolution combinations.

•Single-bit noise shaping D/A with semi-digital FIR reconstruction filter gaining in popularity for low-end consumer applications.

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Applications (2)

Communications Systems:

•Embedded mixed-signal SOC's: Delta-Sigma ADC's and DAC's found in modem, audio, PLL functions

Major Applications:

•Wireless:

- Cellular: every phone!
  - Qualcomm, Texas Instruments, Nokia/STMicro, Broadcom using $\Delta\Sigma M$ in audio and modem sections
- Bluetooth and WiFi – all using $\Delta\Sigma M$ ADC's.

•Wireline: Cable Modem and DSL chipset providers all using $\Delta\Sigma M$

Stand-Alone Delta-Sigma Converters

•24-bit $\Delta\Sigma M$ ADC's for DC instrumentation and measurement

•National Semi has launched a high-speed continuous-time $\Delta\Sigma M$ chip, but the application is "looking for a home." SOC's still rule by volume.

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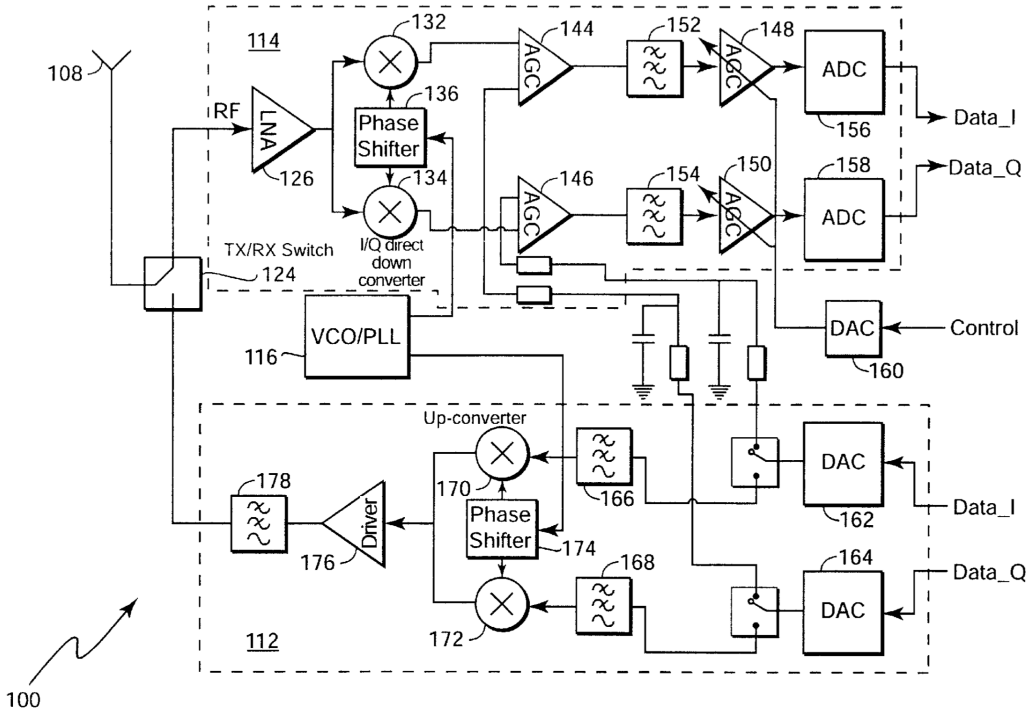
Applications: Digital Radio Modem

Example: First Single-Chip Digital Radio Modem

First Silicon 1999. Initiated/led by Norsworthy at Silicon Wave. Integrates a DEM-based Delta-Sigma A/D with a direct conversion RF front end. DEM is a 'tree structure' from Galton. Key designers listed in patent. Patent now owned by Qualcomm. A de facto Bluetooth architecture.



(10) **Patent No.: US 6,366,622 B1**

(45) **Date of Patent: Apr. 2, 2002**

(54) **APPARATUS AND METHOD FOR WIRELESS COMMUNICATIONS**

(75) Inventors: **Stephen Joseph Brown**; **Andrew Xavier Estrada**, both of San Diego; **Terrance R. Bourk**, La Jolla; **Steven R. Norsworthy**, Solana Beach; **Patrick J. Murphy**; **Christopher Dennis Hull**, both of San Diego; **Glenn Chang**, Laguna Niguel; **Mark Vernon Lane**, San Diego; **Jorge A. Grilo**, Foothill Ranch, all of CA (US)

(73) Assignee: **Silicon Wave, Inc.**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/305,330**

(22) Filed: **May 4, 1999**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/216,040, filed on Dec. 18, 1998, now abandoned.

(51) **Int. Cl.**[7] **H04B 1/30**; H04L 27/18

(52) **U.S. Cl.** **375/322**; 375/133; 375/222; 375/281; 375/345; 329/304

(58) **Field of Search** 375/132, 133, 375/136, 219, 222, 259, 279, 281, 316, 326, 327, 329, 332, 345; 329/304, 306, 307, 308; 455/234.1, 257, 276.1

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,144,308 A 9/1992 Norsworthy 341/131

(List continued on next page.)

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Mixed-Signal SOC Integration:
Examples of Major Management Misses

Management Statements:

- 1985: "A 15MHz switched-capacitor ΔΣM will not work. You will get killed by charge feed-through and noise."
- 1987: "The ΔΣ technique may never get commercialized; not cost effective; too many challenges…"
- 1988: "We will never be able to integrate a DSP with a data converter; not cost effective; too many challenges; too much DSP noise into the codec; double-poly CMOS too costly, penalizes DSP cost…."

- **Fact:**
  - 1989-92: The first ΔΣ voice-band codec; the first single-chip ISDN modem, ΔΣ integrated; the first DSP with integrated ΔΣ codec; first single-chip GSM vocoder, ΔΣ integrated; first single-chip V.34 modem, ΔΣ integrated

Management Statements:

- 1994: "Cannot make cost-effective mixed-signal CMOS SOC's: split off the digital and analog into separate chips; analog real estate too costly; mixed-signal testing too costly; double poly process too costly; low voltage digital process not allowing enough headroom for analog signals; too much noise from digital; too much substrate bounce."

- **Fact:**
  - Multi-billion-dollar mixed-signal CMOS SOC worldwide market; billions of consumers worldwide using every day.

Management Statements:

- A Bluetooth startup in 1999: "Bluetooth will be 2-chip solution: a radio chip and a separate microcontroller; too many technical challenges integrating RF with microcontroller; cannot be done in CMOS; too costly to integrate, test and produce; microcontroller licensing cost too high; firmware support for microcontroller too costly."

- **Fact:**
  - First movers on single-chip CMOS Bluetooth SOC's took market share quickly, some went IPO successfully. Those who didn't integrate to a single chip early were late to the party when the market forced them to do so, and some dissolved their organizations as a result.

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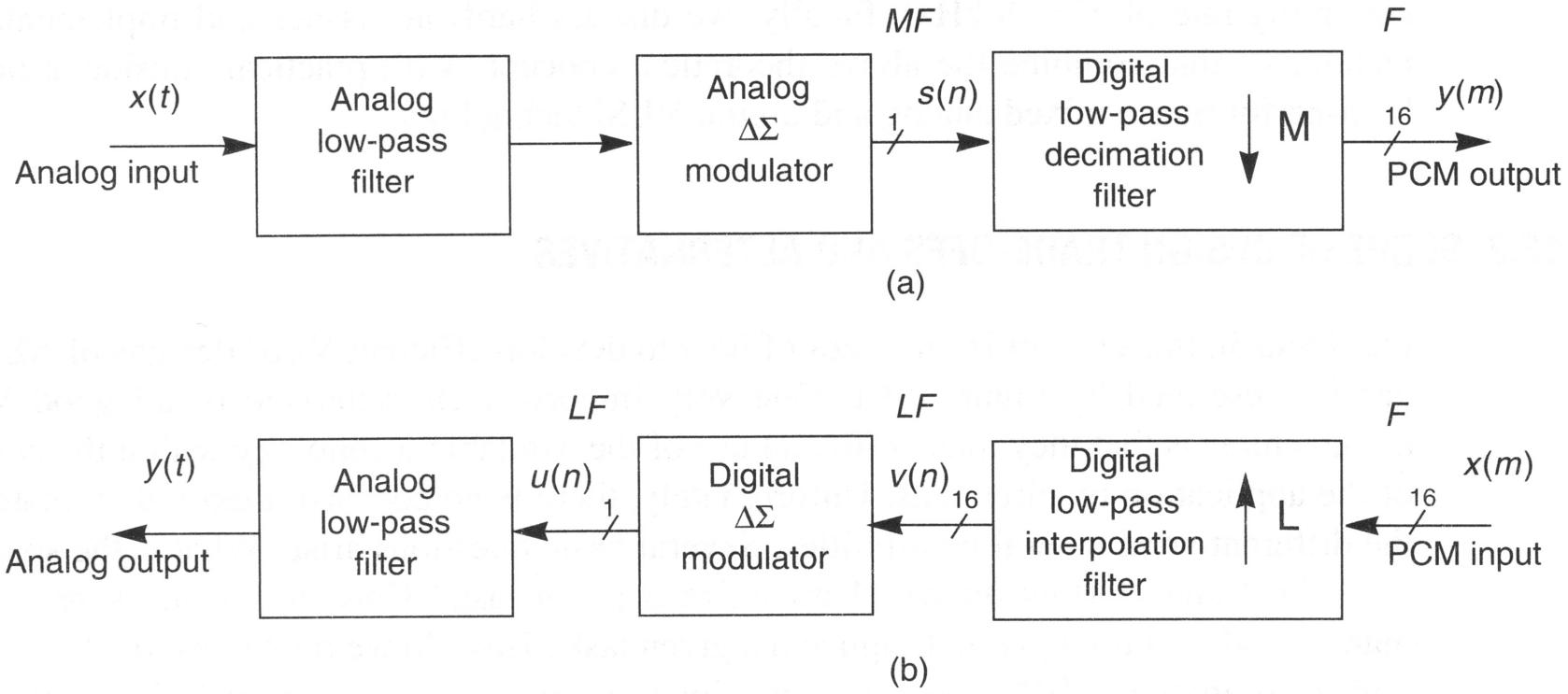
Decimation and Interpolation for Delta-Sigma Conversion



(a) A ΔΣ A/D converter system; (b) ΔΣ D/A converter system.

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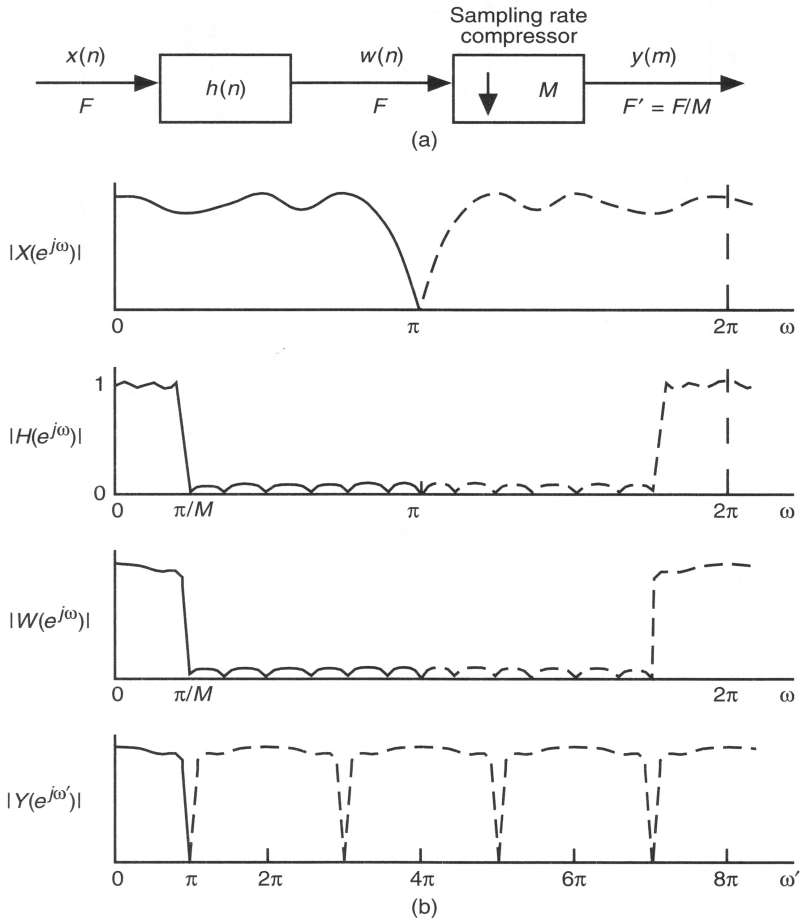
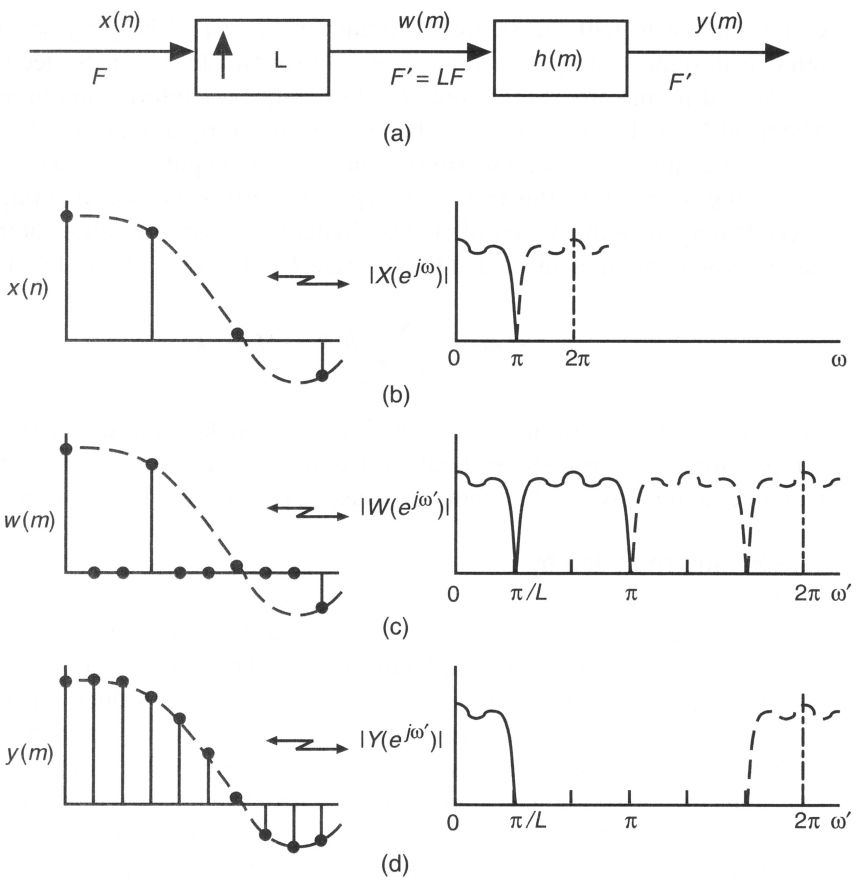
Decimation and Interpolation



(a) Block diagram and (b) typical spectra for decimation by an integer factor M.



(a) Block diagram and (b) typical waveforms and spectra for interpolation by an integer factor L.

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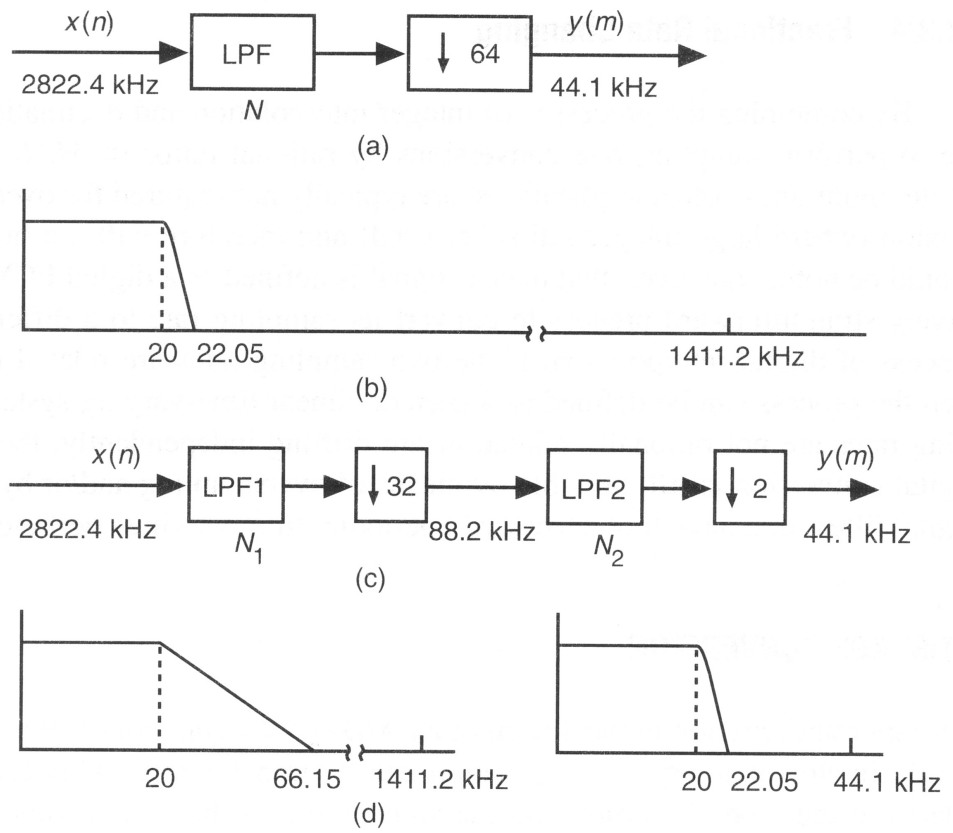
Multistage Decimation or Interpolation

Breaking up into multiple stages results in dramatic efficiency improvements



Simple example of a one-stage and a two-stage network for decimation by a factor of 64 to 1.

Requires 6250-tap filter and 138 X 10^6 multiplies / sec.

Requires N_1=291 and N_2=205 taps and only 17 X 10^6 multiplies / sec.

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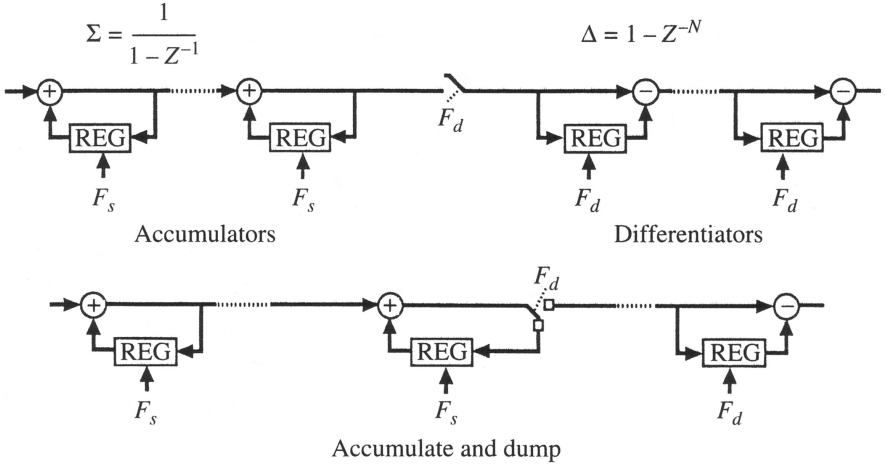
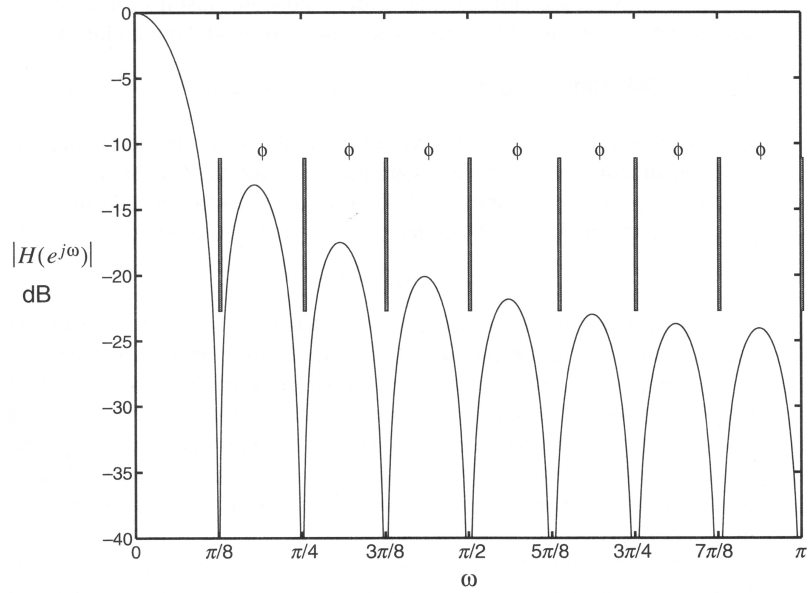
sinc^K Filtering (1)



A sinc^K decimating circuit that comprises K accumulators, followed by resampling and K differentiators. All additions are performed modulo 2^b, b being the number of bits required in the output word. The second circuit resamples using an accumulate-and-dump circuit.



Frequency response of sinc^3 filter with M = 16, showing "don't care" bands.

$$H(z) = \left(\frac{1}{M}\,\frac{1 - z^{-M}}{1 - z^{-1}}\right)^K$$

and its frequency response is therefore

$$|H(e^{j\omega})| = \left(\frac{1}{M}\,\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right)^K$$

where

$$\omega = 2\pi f/f_s$$

It has $M/2$ spectral zeros if M is even, or $\lceil M/2 \rceil - 1$ if M is odd, at frequencies that are multiples of the decimated sampling frequency ω_d, that is,

$$H(e^{j\omega}) = 0 \qquad \omega = n\omega_d \qquad n = \{1, 2, 3, \ldots, \lfloor M/2 \rfloor\}$$

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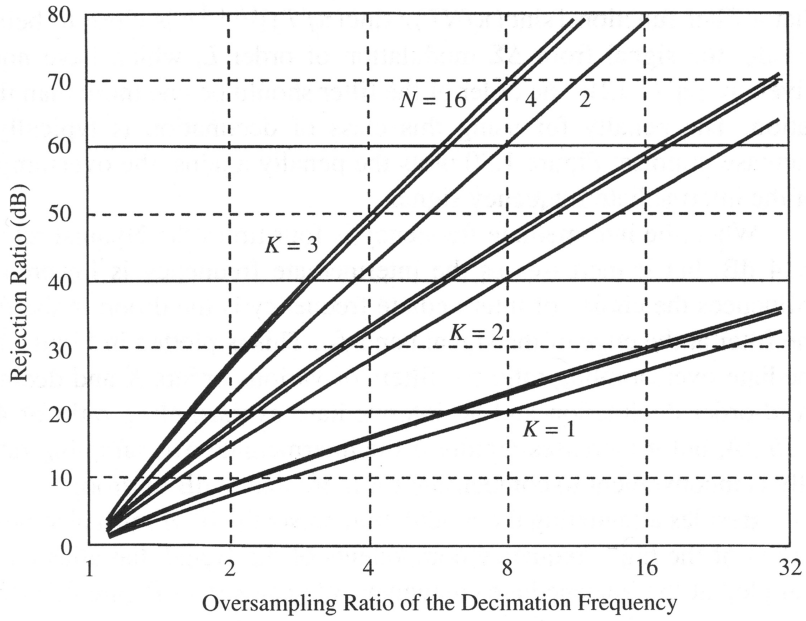
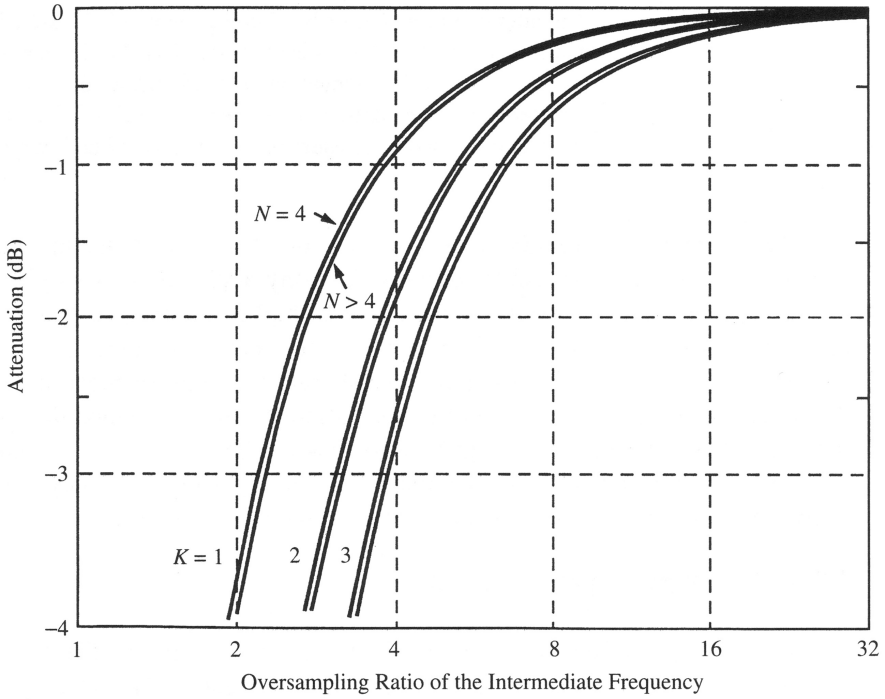
sinc^K Filtering (2)



A graph of

$$\frac{\text{sinc}^k\{\pi(f_D - f_0)NT\}}{\text{sinc}^k\{\pi(f_D - f_0)T\}}$$

It is attenuation of out-of-band components of the signal at frequency $f_D - f_0$ for sinc^k decimation; N is the decimation ratio $N = f_s/f_D$. This attenuation should meet the antialiasing requirement of the application.



Attenuation of sinc^k decimation filters at the edge of the signal band, f_0. This amount of droop in the signal needs to be compensated.

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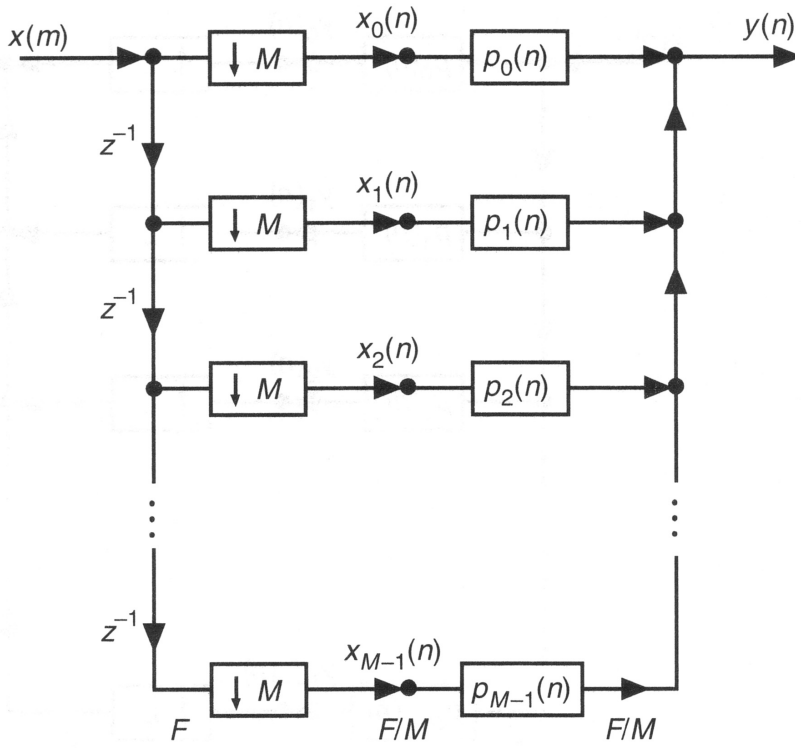
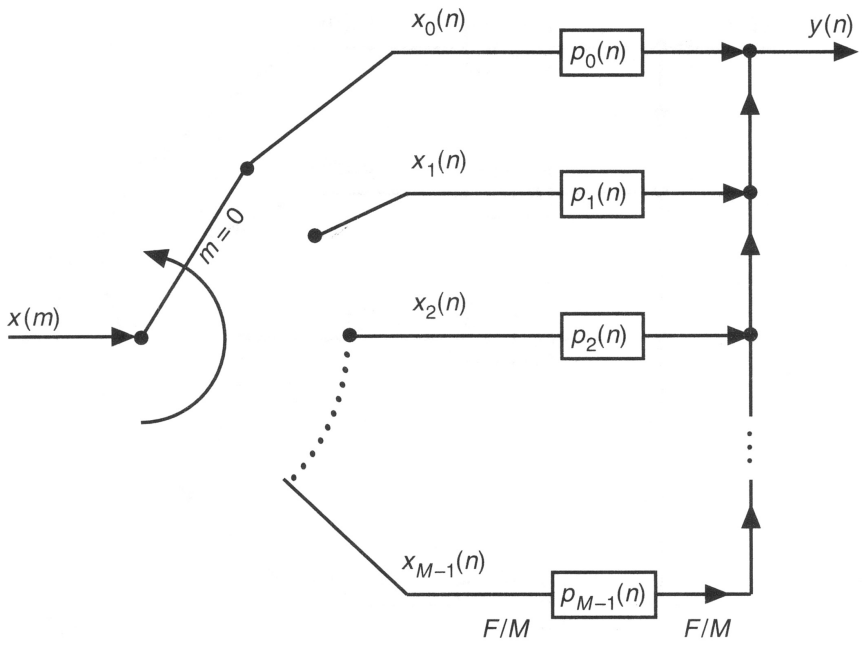
Polyphase Decimators

A factor of M (or L) in savings of computational rate is achieved by performing the filtering operations at the low rate side of the structure rather than on the high rate side.



Polyphase structure for an M-to-1 decimator.



Counterclockwise commutator model for an M-to-1 decimator.

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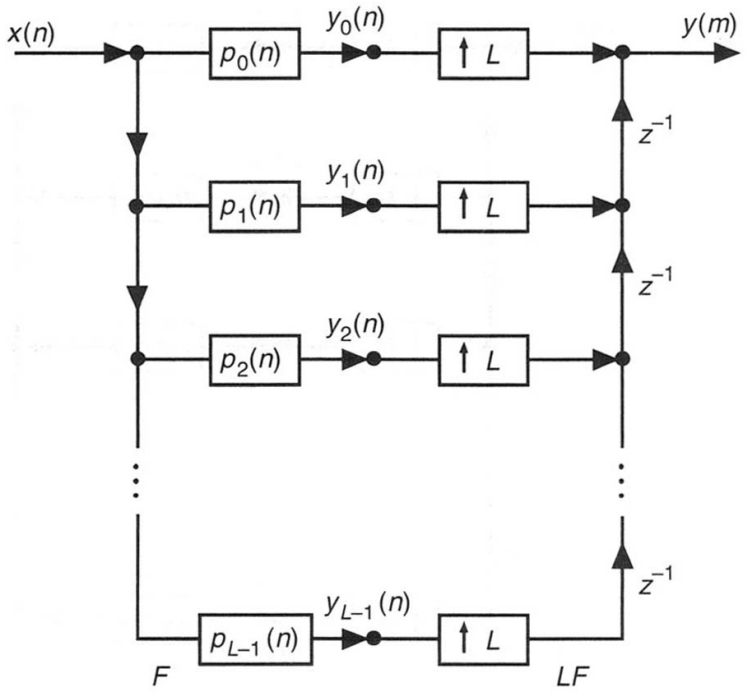
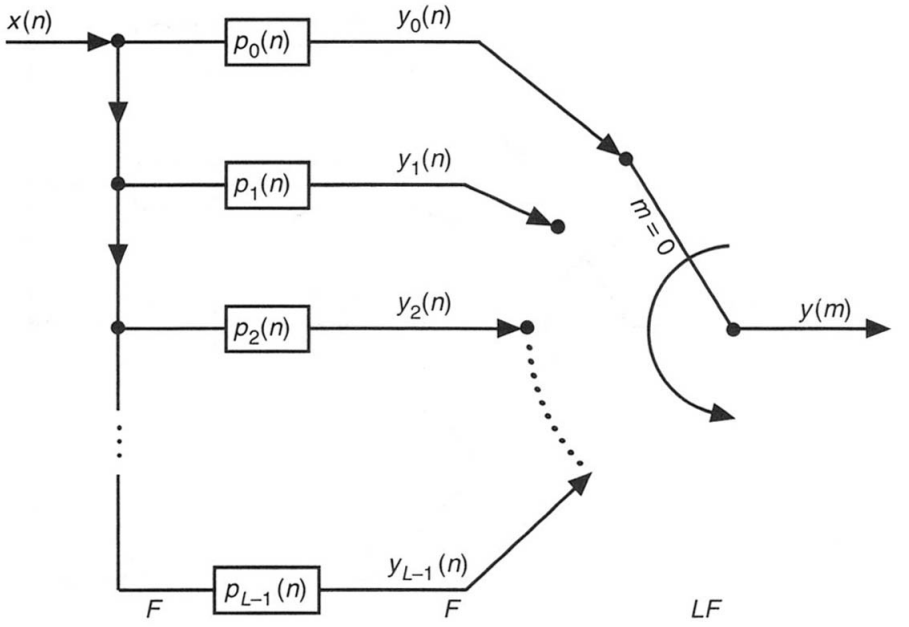
Polyphase Interpolators

A factor of M (or L) in savings of computational rate is achieved by performing the filtering operations at the low rate side of the structure rather than on the high rate side.



Polyphase structure for a 1-to-L interpolator.



Counterclockwise commutator model for a 1-to-L interpolator.

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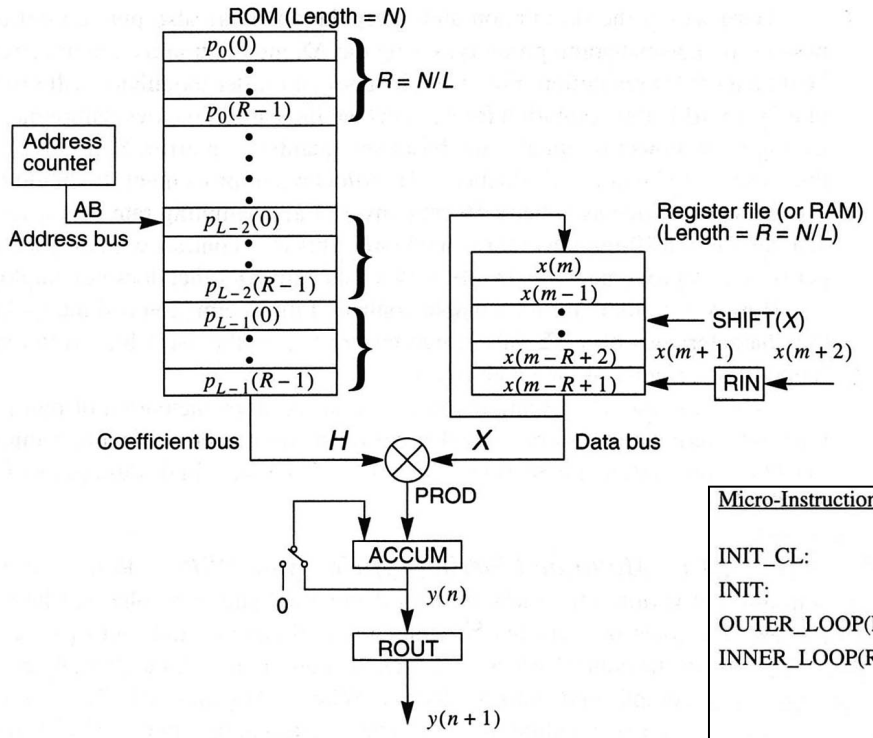
Polyphase Interpolator Example



Example of an custom ALU-based hardware polyphase interpolator with micro instruction sequence.

Micro-Instruction Sequence

```
INIT_CL:          CLEAR(ACCUM);                 /* The first clearing of the accumulator */
INIT:             AB = N-1;                     /* Initialize address counter every N */
OUTER_LOOP(L):    FOR(n = 0; n < L-1; n++) {    /* Do outer loop L times */
INNER_LOOP(R):        FOR(r = 0; r < R-1; r++) {  /* Do inner loop R = N/L times */
                          PROD = H * X;         /* First multiply is p_{L-1}(R-1) * x(m-R+1) */
One cycle                 ACCUM += PROD;        /* Multiply/accumulate */
                          AB --;                /* Decrement address counter */
                          SHIFT(X);             /* Shift the register file */
                      }                         /* End inner loop */
                      LOAD(ROUT);               /* New output y(n) */
                      CLEAR(ACCUM);             /* Clear the accumulator */
                  }                             /* End outer loop */
                  LOAD(RIN);                    /* Load new x(m) and overwrite x(m-R+1) */
                  SHIFT(X);                     /* Shift new x(m) to top of stack */
RETURN:           GOTO(INIT);                   /* Return to top; compute next L outputs */
```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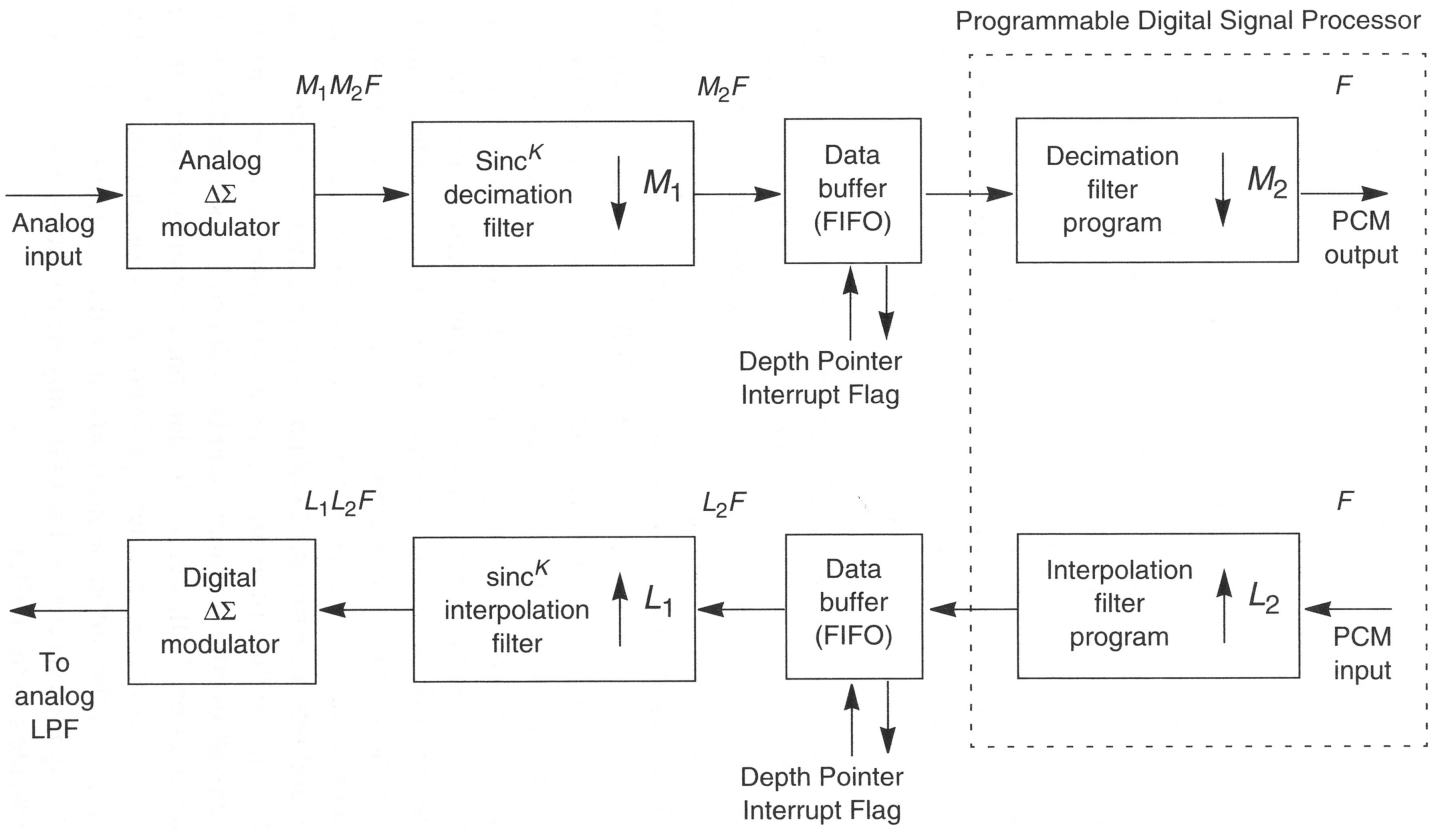
Modern Architecture of ΔΣM and DSP



Multistage decimator and interpolator incorporating a programmable DSP with data buffering between stages.

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Current Problems and New Applications

- Pushing into areas occupied by pipelined A/D converters (e.g., using a very low oversampling ratio with ENOB ≥ 12)
- Medical imaging, requiring massive parallelism (hundreds of converters and DSP's in a small area)
- Lowering the phase noise of $\Delta\Sigma$-based fractional-N PLL's
- Direct RF-to-Digital conversion: RF_2Bits and $Bits_2RF$.
- Software-defined radio.
- Programmable data conversion – DSP system on a chip that trades off resolution for bandwidth.

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